Proceedings of the 26th International Conference on Electrical Machines and Systems (ICEMS 2023),
Zhuhai, China, November 5-8, 2023

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***Abstract*—Charging stations for electric vehicles require electrical isolation between the charging ports. Therefore, this paper proposes a multi-port DC/DC converter structure that combines three conventional dual-active bridge converters (DABCs) where the primary side switching stages are integrated into a single four-leg inverter, and three individually isolated output ports (4L3) are provided. This quad-active bridge converter (QABC) structure features fewer semiconductor devices than three parallel connected single-phase DABCs with a six-leg inverter (3×2L3, resulting in 6L3). The 4L3 QABC is also advantageous compared to a known variant where the primary side switching stages are integrated into a three-leg inverter (3L3), as the 4L3 QABC does not limit the duty cycles of the primary side transformer voltages. Therefore, the input voltage can be fully utilized, which allows lower transformer RMS currents compared to the conventional 3L3 QABC. Our analysis explains the operation and modulation and underscores the 4L3 QABC's enhanced performance that consistently diminishes transformer current across all operational ranges, achieving a 20 % reduction in the sum of squared transformer RMS currents at rated operation compared to the conventional 3L3 QABC. Furthermore, we show a virtual prototype with an integrated cooling system, which reaches a power conversion efficiency of 98.4 % for 750 V/400 V primary/secondary voltages at 120 kW and a power density of 10 kW/dm^3.**

***Index Terms*—Multi-Port Converter, Charging System, DAB, Dual Active Bridge, DC/DC Converter, Four-Leg Inverter.**

I. Introduction

Insulated multi-port DC/DC converters are becoming increasingly important in electric vehicle (EV) charging stations and renewable energy sources due to their ability to manage multiple power flows while maintaining high efficiency and reliability. Conventional charging stations are typically connected to a medium-voltage AC supply via a low-frequency transformer, which steps down the AC voltage to typically 400 VAC. This voltage is converted to a 750 V DC voltage by a large power factor correction (PFC) rectifier [1]. The DC output from the front-end PFC rectifier is distributed across the entire charging station, providing an opportunity to connect to local photovoltaic (PV) systems and a central energy buffer battery [2]. This setup also allows for managing power peaks at individual charging ports, ensuring a stable power supply. However, each charging port needs to be isolated from the others [3] and must be capable of high efficiency and adaptability to voltage variations attributed to the state of charge (SoC) of the batteries. In order to meet these requirements, numerous studies have been conducted on topologies based on the Dual Active Bridge (DAB) structure, given its properties such as isolated bidirectional power flow with high control dynamics and soft switching in certain operational areas [4]–[11].

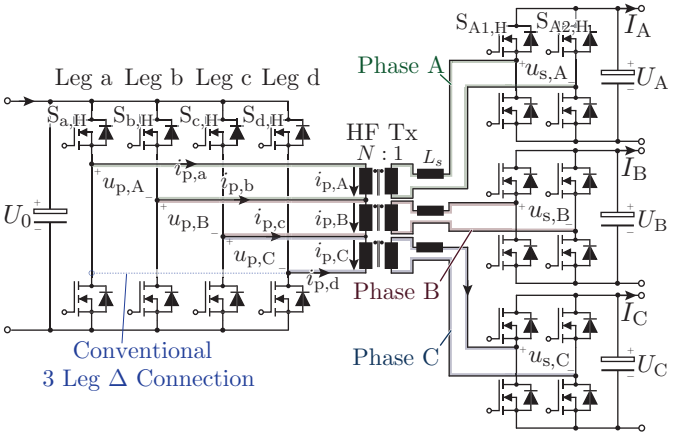


Fig. 1: Proposed multi-port DC/DC converter topology formed by integrating the primary converter stages of three dual active bridge converters (DABCs) into a four-leg inverter. The resulting topology is named 4L3 QABC, indicating three controllable DC outputs operated by three independent DABCs, abbreviated as phases A, B, and C. The dotted line denotes the known three-leg inverter topology (3L3 QABC), as referenced in [12], [13].

One such four-port structure is based on the integration of three DAB converters (DABCs) [12], which is composed of a three-phase inverter on the primary side, three single-phase inverters on the secondary side, and three independent high-frequency (HF) transformers (3L3). The transformer terminals on the primary side are delta-connected (see the blue dotted line in **Fig. 1**), which allows impressing each transformer's primary voltage as the difference of two neighboring bridge-legs' output voltages. However, this 3L3 structure limits the sum of the transformer primary voltage duty cycles to ≤ 2 [12], [13]. This constraint not only leads to decreased DC-link voltage utilization and increased transformer RMS currents but also prevents improved operation, like soft switching through duty cycle control.

Therefore, this paper proposes a topology that adds an extra bridge-leg to the primary side of the 3L3 structure, resulting in the proposed 4L3 structure shown in **Fig. 1**. The 4L3 structure enables independent generation of the three transformer primary voltages. In particular, the novel topology can output full-duty-cycle voltages on all phases of the primary side, thereby reducing transformer RMS currents. Furthermore, through the independent operation of the three

TABLE I: Specifications and component values of the 4L3 QABC.

Given parameters	
Nominal primary side DC voltage	$U_0 = 750\,\mathrm{V}$
Nominal secondary side DC voltages	$U_\mathrm{A} \approx U_\mathrm{B} \approx U_\mathrm{C} \approx 400\,\mathrm{V}$
Nominal power	$3 \times 40\,\mathrm{kW}$
Secondary side current limit	$I_{\{\mathrm{A,B,C}\},\mathrm{max}} = 100\,\mathrm{A}$
Secondary side voltage limit	$U_{\{\mathrm{A,B,C}\},\mathrm{max}} = 450\,\mathrm{V}$
Switching frequency	$f_\mathrm{s} = 20\,\mathrm{kHz}$
Derived parameters	
Transformer's turns ratio	$N = 15/8$
Transformer's stray inductance	$L_\mathrm{s} = 17.9\,\mu\mathrm{H}$

parallel DABCs of the 4L3 QABC, abbreviated as phases A, B, and C in **Fig. 1**, modulation methods for single-phase DABC can be independently applied to each phase aimed at suppressing reactive current and achieving soft switching. This paper explains the operation and modulation concepts of the 4L3 QABC, revealing the advantages of the additional leg through comparison with 3L3 QABC. Additionally, it analyzes the characteristics of the 4L3 QABC in an example application of a $400\,\mathrm{V}$ $120\,\mathrm{kW}$ EV charger, with the operational voltages and currents being determined as shown in **Tab. I**. **Sec. II** introduces the operational principle of the 4L3 QABC and specifies the modulation parameters available for converter control. **Sec. III** analyzes the current stress of the legs of the four-leg inverter and compares the transformer current stress of the proposed 4L3 QABC and the conventional 3L3 QABC. In **Sec. IV**, the 4L3 QABC stationary battery charger design and performance are described. **Sec. V** concludes the paper.

II. Operation and Modulation of the 4L3 QABC

The investigated 4L3 QABC (cf. **Fig. 1**) has three HF transformers, whose primary windings are connected in an *open delta* configuration and supplied with a four-leg two-level inverter, as depicted in **Fig. 1**. Each of the three secondary windings is connected to a full-bridge converter that transmits power to the isolated output ports. In the following, we explain the 4L3 QABC's operating principle and used modulation schemes. Note that indexes with lower-case letters $\mathrm{a}, \mathrm{b}, \mathrm{c}$ and d are used for quantities directly related to the four primary side bridge-legs and indexes with upper-case letters A, B and C are used for quantities directly related to the three phases.

A. Operating Principle

In **Fig. 2(a)**, generation of the primary side voltages $u_{\mathrm{p,A}}$, $u_{\mathrm{p,B}}$, $u_{\mathrm{p,C}}$ from the high-side gate driver signals $\mathrm{S_{a,H}}$, $\mathrm{S_{b,H}}$, $\mathrm{S_{c,H}}$, $\mathrm{S_{d,H}}$, is explained. As indicated in **Fig. 2(a)**, the primary side voltages are controlled by the duty cycles $D_{\mathrm{p,A}}$, $D_{\mathrm{p,B}}$, and $D_{\mathrm{p,C}}$, which are controlled by the phase shift between the primary side gate signals. More specifically, $D_{\mathrm{p,A}}$ is determined by the phase shift between $\mathrm{S_{a,H}}$ and $\mathrm{S_{b,H}}$, $D_{\mathrm{p,B}}$ is determined by the phase shift between $\mathrm{S_{b,H}}$ and $\mathrm{S_{c,H}}$, and $D_{\mathrm{p,C}}$ is determined by the phase shift between $\mathrm{S_{c,H}}$ and $\mathrm{S_{d,H}}$. Therefore, the 4L3 QABC can generate any duty cycle for the primary side voltages without coupling between the phases, like the 6L3 DABC that uses six legs (three full bridges) on the primary side. A limitation of the 4L3 QABC compared to the 6L3 DABC is the inability to control the phase shifts between the primary side voltages $u_{\mathrm{p,A}}$, $u_{\mathrm{p,B}}$, $u_{\mathrm{p,C}}$. Namely, the 4L3 QABC's legs 'b' and 'c' generate the two adjacent output voltages and can fully control the duty cycles $D_{\mathrm{p,A}}$, $D_{\mathrm{p,B}}$ and $D_{\mathrm{p,C}}$, but, consequently, not the phase shift between them. This limitation does not influence the power transfer of the 4L3 QABC but limits its capability to minimize the current stress of the primary side dc capacitor.

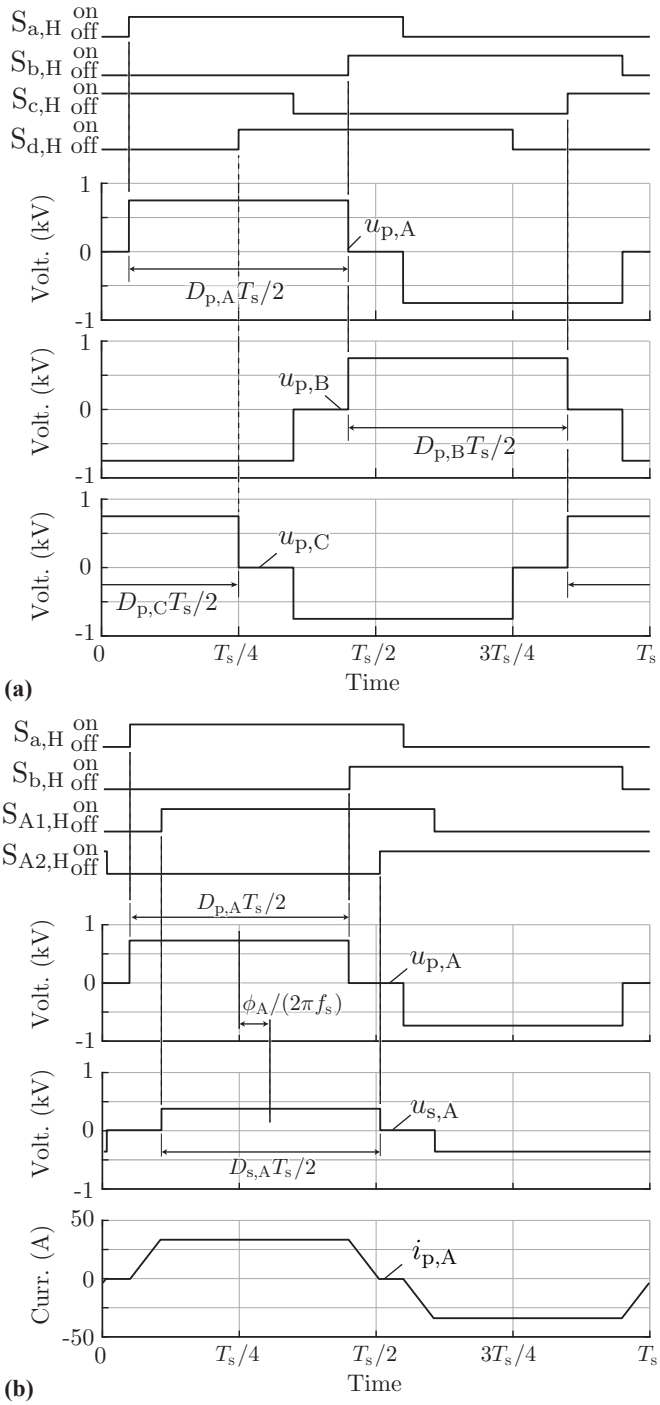


Fig. 2: Typical operation waveforms of the 4L3 QABC when all duty cycles are set as $D_{\{\mathrm{p,s}\},\{\mathrm{A,B,C}\}} = 0.8$, and phase shifts are set as $\phi_{\{\mathrm{A,B,C}\}} = \pi/9$: **(a)** Gate signals of the high-side of the four-leg inverter and its output voltages to the primary side terminals of the HF transformers. **(b)** Gate signals, imposed voltages to the primary and secondary side terminals of the HF transformers, and the transformer current of phase A of the 4L3 QABC.

The primary side and the secondary side voltages, and the primary current of the phase A, i.e., $u_{\mathrm{p,A}}$, $u_{\mathrm{s,A}}$ and $i_{\mathrm{p,A}}$, are depicted in **Fig. 2(b)**. Secondary side voltage $u_{\mathrm{s,A}}$ with arbitrary duty cycle $D_{\mathrm{s,A}}$ and phase shift ϕ_A between the

primary side voltage $u_{\mathrm{p,A}}$ can be generated by an independent full-bridge converter on the secondary side with high-side gate signals $\mathrm{S_{A1,H}}$ and $\mathrm{S_{A2,H}}$. When applying these voltages over the transformer's stray inductance, with an arbitrary combination of duty cycles and phase shift represented as $(D_{\mathrm{p,A}}, D_{\mathrm{s,A}}, \phi_{\mathrm{A}})$, the primary side transformer current $i_{\mathrm{p,A}}$ is formed. Consequently, the power P_{A} is transmitted from the primary to the secondary side (in phase A) of the 4L3 QABC, similar to a single-phase DABC. Since all secondary side full-bridges can operate independently, phases B and C of the 4L3 QABC operate in the same manner as phase A.

B. Modulation

The modulation of the 4L3 QABC aims to determine the combination of nine parameters: the three primary side duty cycles $D_{\mathrm{p,\{A,B,C\}}}$, the three secondary side duty cycles $D_{\mathrm{s,\{A,B,C\}}}$, and the three phase shifts between the primary side and secondary side voltages $\phi_{\mathrm{\{A,B,C\}}}$, cf. **Fig. 2(b)**. Each parameter combination is obtained to provide the desired power level per phase $P_{\mathrm{A}}, P_{\mathrm{B}}, P_{\mathrm{C}}$ to each load at the voltage $U_{\mathrm{A}}, U_{\mathrm{B}}, U_{\mathrm{C}}$.

As mentioned in **Sec. II-A**, each phase of the 4L3 QABC operates equivalently to a single-phase DABC. Therefore, the modulation of each phase can be designed individually and in the same manner as for a single-phase DABC. Various modulation techniques for single-phase DABC have been proposed with the objectives of reducing reactive power, achieving soft-switching, ensuring smooth transitions between modulation methods, and simplifying implementation [14]–[23]. Therefore, to achieve these objectives, in this paper, single phase shift (SPS), dual phase shift (DPS) proposed in [19], and triangular current modulation (TCM) are employed for the 4L3 QABC.

When the power level of the phase is low, TCM is used to reduce reactive power. In TCM, the transformer is excited by the primary side voltage first, and a triangular current is generated using the voltage difference between the primary side and the secondary side. TCM is employed up to a power level threshold represented as

$$\begin{aligned} P_{\mathrm{TCM}} &= \frac{U_{\mathrm{\{A,B,C\}}}^2 (1-d)}{4 f_{\mathrm{s}} L_{\mathrm{s}}}, \qquad \text{for } d \le 1 \\ P_{\mathrm{TCM}} &= \frac{(U_0/N)^2 (1-1/d)}{4 f_{\mathrm{s}} L_{\mathrm{s}}}, \quad \text{for } d > 1 \end{aligned} \tag{1}$$

where $d = NU_{\mathrm{\{A,B,C\}}}/U_0$ represents the voltage ratio between the primary and secondary, taking into account the transformer's turns ratio N [24]. When the duty cycle of either the primary or secondary side voltage approaches 1, the power level reaches the threshold of TCM, prompting a transition to DPS.

The DPS proposed in [19] is derived to minimize reactive current while maintaining zero voltage switching (ZVS) and ensuring a smooth parameter transition to both TCM and SPS. When both the primary and secondary side voltage duty cycle reach 1, the power level reaches the DPS threshold represented as

$$\begin{aligned} P_{\mathrm{DPS}} &= \frac{U_0 U_{\mathrm{\{A,B,C\}}} (1-d^2)}{8 f_{\mathrm{s}} L_{\mathrm{s}} N}, \qquad \text{for } d \le 1 \\ P_{\mathrm{DPS}} &= \frac{U_0 U_{\mathrm{\{A,B,C\}}} \left(1-1/d^2\right)}{8 f_{\mathrm{s}} L_{\mathrm{s}} N}, \quad \text{for } d > 1 \end{aligned} \tag{2}$$

and the modulation transits to SPS [19].

In SPS, the primary and secondary duty cycles are fixed at 1, and power transmission is performed by only adjusting phase shifts ϕ_{A}, ϕ_{B}, and ϕ_{C}. The duty cycles and phase shifts for each modulation method are summarized in **Tab. II**. Due to its very long analytic expression, the complete expression for the parameter m is omitted here, and it can be found in [19].

Fig. 3(a) illustrates the relationship between the power level thresholds (1), (2) and the operating range of the charging system with the specifications given in **Tab. I**. The operating points of each phase of the 4L3 QABC are represented by three arbitrary points on the SoC, indicated by the blue line **Fig. 3(a)**, and the corresponding modulation method is applied for each operating point. **Fig. 3(b)** shows the transformer imposed voltage and transformer current of the 4L3 QABC as an example when each phase is positioned at different operating points indicated in **Fig. 3(a)**.

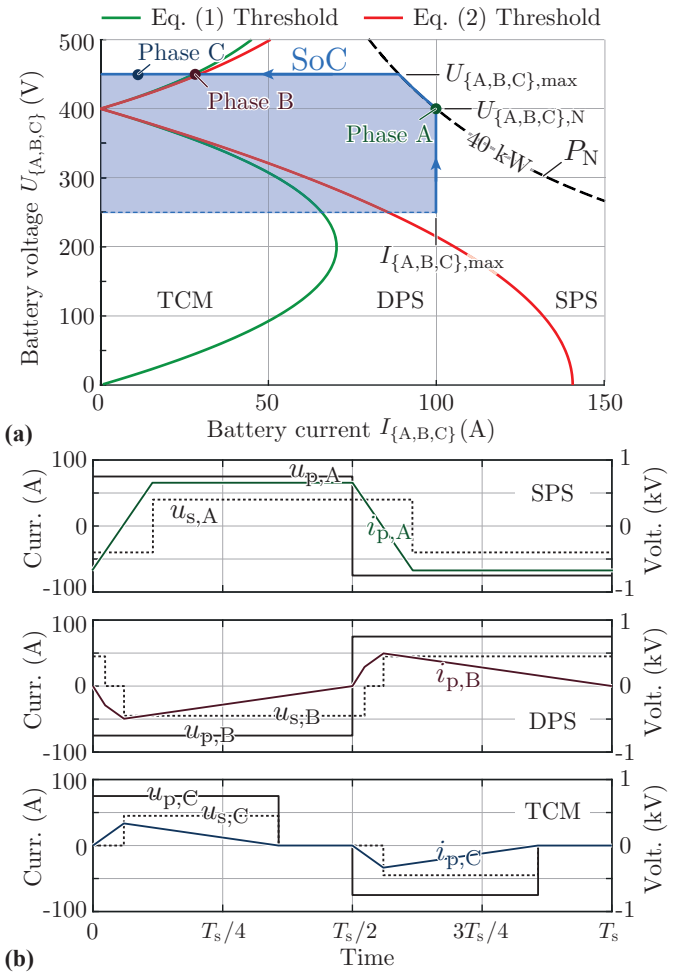


Fig. 3: Modulation and waveforms of the 4L3 QABC in the whole operational area: **(a)** Modulation boundaries and operational points on the SoC, based on **Tab. I**, as indicated by equations (1) and (2). Three characteristic waveforms are shown in **(b)** related to arbitarily selected operational points of the phases A, B, and C of the 4L3 QABC on the SoC. **(b)** Current and voltage waveforms of each phase of the 4L3 QABC. SPS, DPS, and TCM are selected as demonstrations of waveforms on the SoC for each phase, respectively, as shown in **(a)**.

TABLE II: Phase-shift combination for the 4L3 QABC in each power level

$d \leq 1$ **Buck mode**	**TCM:** $0 < P < P_{\mathrm{TCM}}$	**DPS:** $P_{\mathrm{TCM}} \leq P \leq P_{\mathrm{DPS}}$	**SPS:** $P_{\mathrm{DPS}} < P$
$\phi_{\{\mathrm{A,B,C}\}}$	$\pi\sqrt{f_{\mathrm{s}}L_{\mathrm{s}}\frac{U_0/N-U_{\{\mathrm{A,B,C}\}}}{U_{\{\mathrm{A,B,C}\}}^2 U_0/N}P}$	$\frac{\pi}{2}-\frac{\sqrt{2m(\pi dU_0/N)^2-(m\pi dU_0/N)^2-8\pi^2 df_{\mathrm{s}}L_{\mathrm{s}}P}}{2dU_0/N}$	$\frac{\pi}{2}\left(1-\sqrt{1-\frac{8f_{\mathrm{s}}L_{\mathrm{s}}P}{U_0U_{\{\mathrm{A,B,C}\}}/N}}\right)$
$D_{\mathrm{p},\{\mathrm{A,B,C}\}}$	$2\frac{\phi_{\{\mathrm{A,B,C}\}}}{\pi}\frac{U_{\{\mathrm{A,B,C}\}}}{U_0/N-U_{\{\mathrm{A,B,C}\}}}$	m [19]	1
$D_{\mathrm{s},\{\mathrm{A,B,C}\}}$	$2\frac{\phi_{\{\mathrm{A,B,C}\}}}{\pi}\frac{U_0/N}{U_0/N-U_{\{\mathrm{A,B,C}\}}}$	1	1
$d > 1$ **Boost mode**	**TCM:** $0 < P < P_{\mathrm{TCM}}$	**DPS:** $P_{\mathrm{TCM}} \leq P \leq P_{\mathrm{DPS}}$	**SPS:** $P_{\mathrm{DPS}} < P$
$\phi_{\{\mathrm{A,B,C}\}}$	$\pi\sqrt{f_{\mathrm{s}}L_{\mathrm{s}}\frac{U_{\{\mathrm{A,B,C}\}}-U_0/N}{U_{\{\mathrm{A,B,C}\}}(U_0/N)^2}P}$	$\frac{\pi}{2}-\frac{\sqrt{2m(\pi dU_0/N)^2-(m\pi dU_0/N)^2-8\pi^2 df_{\mathrm{s}}L_{\mathrm{s}}P}}{2dU_0/N}$	$\frac{\pi}{2}\left(1-\sqrt{1-\frac{8f_{\mathrm{s}}L_{\mathrm{s}}P}{U_0U_{\{\mathrm{A,B,C}\}}/N}}\right)$
$D_{\mathrm{p},\{\mathrm{A,B,C}\}}$	$2\frac{\phi_{\{\mathrm{A,B,C}\}}}{\pi}\frac{U_{\{\mathrm{A,B,C}\}}}{U_{\{\mathrm{A,B,C}\}}-U_0/N}$	1	1
$D_{\mathrm{s},\{\mathrm{A,B,C}\}}$	$2\frac{\phi_{\{\mathrm{A,B,C}\}}}{\pi}\frac{U_0/N}{U_{\{\mathrm{A,B,C}\}}-U_0/N}$	m [19]	1

III. Operation Characteristics and Comparison to 3L3 QABC

The intended application of the 4L3 QABC is an off-board EV charger, which, depending on the battery's SoC, can have various voltage levels and required charging currents for each output. Therefore, to show the operational performance of the 4L3 QABC under various voltage/current levels, we consider the following two operating cases:

- *Case 1*: Phase B and C are fixed at the rated operational point, and phase A operates at all points below the rated power, i.e.,

$$\begin{aligned}&\{(250\,\mathrm{V} \leq U_{\mathrm{A}} \leq 450\,\mathrm{V},\ 0\,\mathrm{A} \leq I_{\mathrm{A}} \leq 100\,\mathrm{A},\\ &0 \leq P_{\mathrm{A}} \leq 40\,\mathrm{kW}),\\ &(U_{\mathrm{B}} = 400\,\mathrm{V},\ I_{\mathrm{B}} = 100\,\mathrm{A},\ P_{\mathrm{B}} = 40\,\mathrm{kW}),\\ &(U_{\mathrm{C}} = 400\,\mathrm{V},\ I_{\mathrm{C}} = 100\,\mathrm{A},\ P_{\mathrm{C}} = 40\,\mathrm{kW})\}.\end{aligned}$$

- *Case 2*: Phase B and C are fixed at the operational point with half of the rated power with constant voltage (CV), and phase A operates at all points below the rated power, i.e.,

$$\begin{aligned}&\{(250\,\mathrm{V} \leq U_{\mathrm{A}} \leq 450\,\mathrm{V},\ 0\,\mathrm{A} \leq I_{\mathrm{A}} \leq 100\,\mathrm{A},\\ &0 \leq P_{\mathrm{A}} \leq 40\,\mathrm{kW}),\\ &(U_{\mathrm{B}} = 450\,\mathrm{V},\ I_{\mathrm{B}} = 44.4\,\mathrm{A},\ P_{\mathrm{B}} = 20\,\mathrm{kW}),\\ &(U_{\mathrm{C}} = 450\,\mathrm{V},\ I_{\mathrm{C}} = 44.4\,\mathrm{A},\ P_{\mathrm{C}} = 20\,\mathrm{kW})\}.\end{aligned}$$

For the following analysis, the effects of the device on resistance, winding resistance, excitation current of the transformers, and dead time during switching are neglected.

A. Leg Current of the Four-Leg Inverter

To indicate the current burden of each switch in the primary side four-leg inverter, the RMS current of leg currents is analyzed. The relationships between the four-leg inverter leg currents $i_{\mathrm{p},\{\mathrm{a,b,c,d}\}}$ and transformer current $i_{\mathrm{p},\{\mathrm{A,B,C}\}}$ are expressed as

$$\begin{aligned}i_{\mathrm{p,a}} &= i_{\mathrm{p,A}},\\ i_{\mathrm{p,b}} &= -i_{\mathrm{p,A}} + i_{\mathrm{p,B}},\\ i_{\mathrm{p,c}} &= -i_{\mathrm{p,B}} + i_{\mathrm{p,C}},\\ i_{\mathrm{p,d}} &= -i_{\mathrm{p,C}}.\end{aligned} \tag{3}$$

From the above equations, a change in the transformer current, i.e., a change in the power transmission of a certain phase, affects the currents of the two associated legs of the primary side.

Fig. 4 shows the RMS of leg-currents for the four-leg primary side inverter across the SoC for *Case 1*, and respective

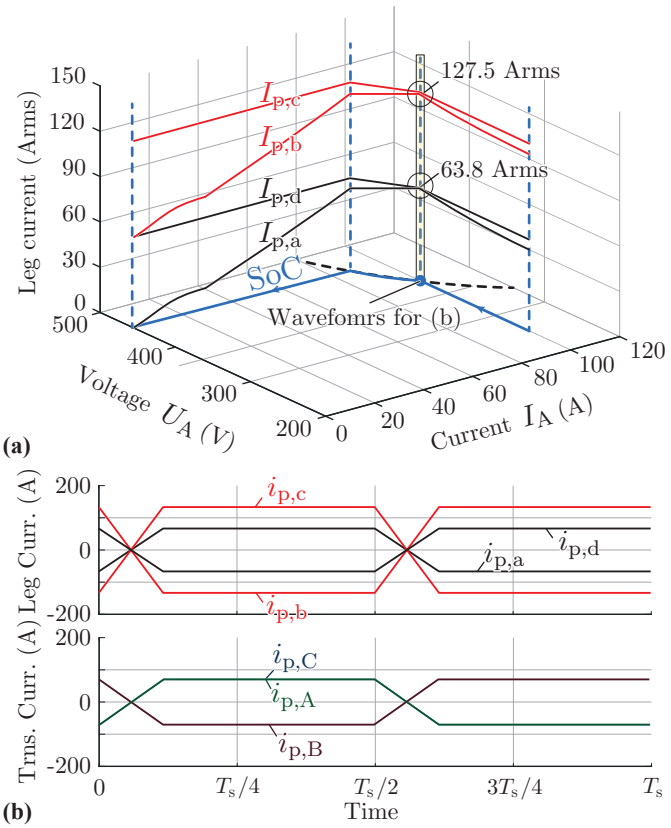


Fig. 4: Four-leg inverter leg current characteristics under *Case 1*: **(a)** Current RMS value of the leg current across the SoC. **(b)** Leg currents $i_{\mathrm{p},\{\mathrm{a,b,c}\}}$ and transformer currents $i_{\mathrm{p},\{\mathrm{A,B,C}\}}$ on the primary side at the rated operation for all phases.

time-domain waveforms for the nominal power at maximum current. **Fig. 4(a)** indicates that the current RMS values of legs c and d are not affected by changes in the operation of phase A, which is in agreement with (3). This is the *Case 1* operation, where the power of phases B and C is fixed. As explained in **Sec. II**, the switching action in the inner legs of the four-leg inverter involves two phases, resulting in a phase difference of 180° between phases A and B, as well as phases B and C as shown in **Fig. 4(b)** (see also the connection in the schematic in **Fig. 1**, where leg b switches phases A and B and the leg c switches the phases B and C). This property of the 4L3 QABC is kept for all the operational points over the SoC of phases B and C. Consequently, at the rated operational point, the RMS value of the inner leg current is twice that of the outer leg current as shown in **Fig. 4**.

B. Comparison of Transformer Currents

The comparison of transformer currents between the 4L3 QABC and the 3L3 QABC is conducted to evaluate the impact of the additional leg on the primary side. The 4L3 QABC is modulated as depicted in **Fig. 3(a)** for this comparison, whereas the 3L3 QABC is modulated according to [13]. The latter minimizes the reactive current of the transformers by solving an optimization problem with the sum of the fundamental component of square root transformer current, i.e., $\sum_{\mathrm{x}\in\{\mathrm{A,B,C}\}} I^2_{\mathrm{p,x}}$ as an objective function under a condition where the sum of the duty cycles is constant.

The comparison results are shown in **Fig. 5**, where the ratio of the squared secondary side RMS transformer current sums is used as a comparison criterion between the 4L3 QABC and the 3L3 QABC, and it is given for the *Case 1* and the *Case 2*. These results in colormap and contour lines of **Fig. 5** are relative values with the 3L3 QABC current as a base value, i.e. $\sum_{\mathrm{x}\in\{\mathrm{A,B,C}\}} I^2_{\mathrm{s,x,4L3}} / \sum_{\mathrm{x}\in\{\mathrm{A,B,C}\}} I^2_{\mathrm{s,x,3L3}}$. For the *Case 1* and the *Case 2*, the ratio is < 1 at all operational points, indicating that the 4L3 reduces the copper losses in the transformer compared to the 3L3 due to the additional leg. To illustrate the reason for the difference in current reduction ratios between *Case 1* and *Case 2*, the input parameters and secondary side RMS transformer current at the rated operation in each *case* are shown in **Tab. III**. For the 4L3 QABC, the modulation of each phase does not affect the other phases, resulting in the transformer current of phase A unchanged in either *Case*. On the other hand, in the 3L3, where the sum of the primary side duty cycles is limited to 2 (cf. [13]), the duty cycle $D_{\mathrm{p,A}}$ allocated to phase A changes as the power transmission of phases B and C changes from *Case 1* to *Case 2*. As a result, the transformer current $i_{\mathrm{s,A}}$ of the 3L3 varies even at the same operational point. Furthermore, the performance of the 3L3 is most degraded compared to the 4L3 when all power references

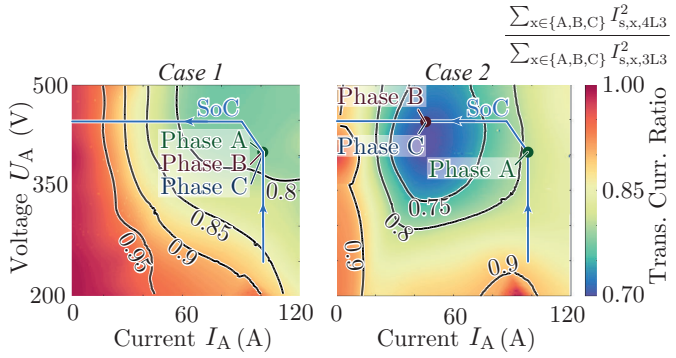


Fig. 5: Ratio of the sum of squares of the transformer secondary side RMS currents comparison between the 4L3 and the 3L3 QABC in *Case 1* and *Case 2*.

TABLE III: Comparison results of input parameters and transformer currents at the rated operation in each *Case*.

		Case 1		*Case 2*	
		4L3	3L3	4L3	3L3
Input parameters	$D_{\mathrm{p,A}}$	1	0.67	1	0.81
	$D_{\mathrm{s,A}}$	1	1	1	1
	ϕ_{A} [rad]	0.73	0.91	0.73	0.80
	$D_{\mathrm{p,B}} = D_{\mathrm{p,C}}$	1	0.67	1	0.59
	$D_{\mathrm{s,B}} = D_{\mathrm{s,C}}$	1	1	1	0.60
	$\phi_{\mathrm{B}} = \phi_{\mathrm{C}}$ [rad]	0.73	0.91	0.28	0.49
Transformer current	$i_{\mathrm{s,A}}$ [Arms]	119.6	135.8	119.6	126.3
	$i_{\mathrm{s,B}}$ [Arms]	119.6	135.8	54.8	70.7
	$i_{\mathrm{s,C}}$ [Arms]	119.6	135.8	54.8	70.7

are the same because the duty cycles can not be larger than 2/3 with an increase in phase shift that takes on the role of the power transmission control instead of the duty cycles.

IV. Design of 4L3 QABC

In this section, the selection of the power semiconductors and the design of the transformer, including a thermal model, are presented. Finally, a virtual 3D CAD prototype and the efficiency of the 4L3 QABC with loss breakdown are given.

To maximize the efficiency and power density, SiC-MOSFETs are employed for the primary side four-leg inverter and the secondary side full-bridge converters. As indicated in **Fig. 4(b)**, the inner legs of the primary side four-leg inverter (leg b and leg c) carry twice the RMS current compared to the outer legs (leg a and leg d) at the rated operation. To select the power semiconductors, in a first approximation, we assume the on-resistance and the thermal resistance scale linearly with the reciprocal of the chip area A, i.e., $R_{\mathrm{on}} \sim A^{-1}$ and $R_{\mathrm{th}} \sim A^{-1}$. Considering only conduction losses, the junction temperature increase is proportional to $\Delta T_{\mathrm{j}} \sim R_{\mathrm{th}} R_{\mathrm{on}} I^2_{\mathrm{semi}}$ and it should be the same for all the semiconductors in the outer and the inner inverter legs. This leads to $\Delta T_{\mathrm{j}} \sim A^{-2} I^2_{\mathrm{semi}}$. To get the same T_{j} for the outer and inner leg semiconductors for twice the RMS current in the inner legs, we must take the inner leg semiconductors with twice the chip area. From the Infineon's catalog, $14\,\mathrm{m\Omega}/1200\,\mathrm{V}$-devices (IMZA120R014M1H) and $7\,\mathrm{m\Omega}/1200\,\mathrm{V}$-devices (IMZA120R007M1H) fit this analysis and, therefore, are suitable for the outer leg and the inner leg semiconductor, respectively. The secondary side employs two $16\,\mathrm{m\Omega}/650\,\mathrm{V}$-devices (C3M0015065K by Cree) in parallel per switch to mitigate the device on-resistance due to the substantial currents compared to the primary side.

The transformer depicted in **Fig. 6** is designed following the Pareto optimization method outlined in [25], [26], which takes into account the proximity effect and skin effect for winding loss, a reluctance circuit model considering fringing, core loss utilizing improved generalized Steinmetz equation [27], [28]. This transformer is composed of N87 Mn-Zn ferrite from TDK. The winding arrangement is configured to provide specific leakage inductance for the DAB operation without an external inductor as

$$0.7 \times L_{\mathrm{s,max}} < L_{\mathrm{s}} < 0.8 \times L_{\mathrm{s,max}},$$
$$\text{where } L_{\mathrm{s,max}} = \frac{\hat{U}_0 U_{\mathrm{dc,N}}}{8 f_{\mathrm{s}} N P_{\mathrm{N}}}. \tag{4}$$

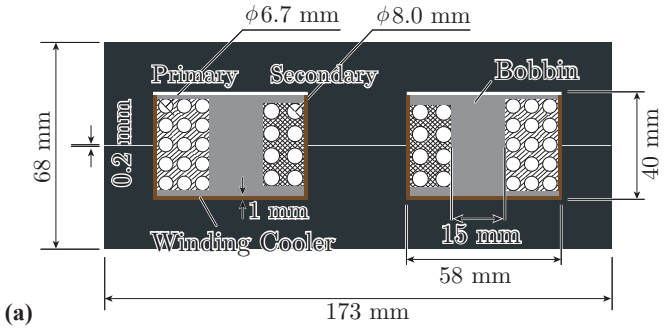
This configuration considers an acceptable increase of the reactive power at the rated power, and it is sensible concerning changing control parameters at low power [8], [13]. Consequently, from the Pareto solutions for efficiency and volume density, considering geometric parameters as optimization variables indicated in **Tab. IV**, a design satisfying the aforementioned leakage inductance was selected in **Fig. 6(a)**. The primary side winding has 15 turns wound in 3 layers, using a litz wire with $4500/71\,\mu\mathrm{m}$ individually isolated strands. Whereas the secondary side winding has 8 turns wound in 2 layers, using a litz wire with $6300/71\,\mu\mathrm{m}$ individually isolated strands. These configurations yield $17.9\,\mu\mathrm{H}$ leakage and $338\,\mu\mathrm{H}$ magnetizing inductance referred to the secondary side with $99.68\,\%$ transformer efficiency. The designed transformer compensates for all the inductance required for DAB operation through leakage inductance, which results in an increased number of windings compared to using an external inductor,

leading to a 0.13 % decrease in transformer efficiency with the same power density, but allowing for a reduction in the number of components and simplification of the cooling system.

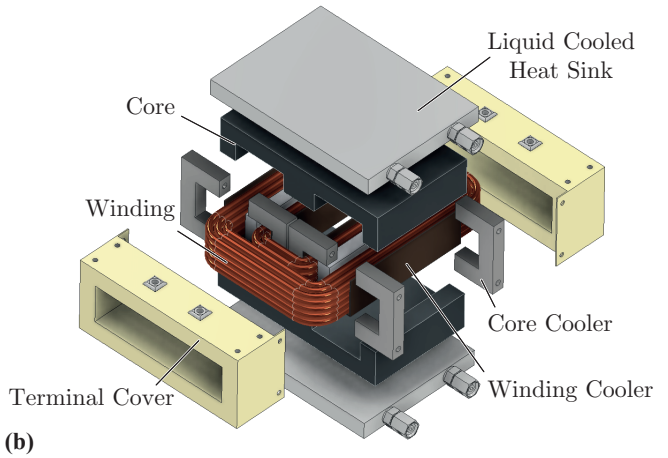
The selected transformer design assumes the cooling system, designed according to [29], and intended to enhance the heat transmission generated from winding losses and core losses through the winding cooler and core cooler, which are made of ceramic metal composite AlSiC-9 to mitigate eddy current losses, to the liquid-cooled heat sink as illustrated in **Fig. 6(b)**. A thermal model of the transformer with the cooling system is established, which allows the selection of the design with the winding hot spot temperature $T_{\rm hs} < 150°$. The hotspot of the winding is located within the winding itself, and it is at the position farthest from each core cooler, as depicted in **Fig.6(c)**. The temperature of the hotspot can be estimated through a thermal equivalent circuit modeling the temperature difference ΔT between the hotspot and the heat sink temperature. The heat flow from the hotspot to the heat sink takes a path that has four directions: (1) radial direction from the winding hotspot towards the winding cooler; (2) axial direction from the winding cooler to the core cooler; (3) radial direction inside of the core cooler; (4) axial direction towards the heat sink as shown in **Fig. 6(c)** according to [29]. Based on this thermal model, the temperature difference between the hotspot and the heat sink can be estimated as

TABLE IV: Optimization parameters for transformer design.

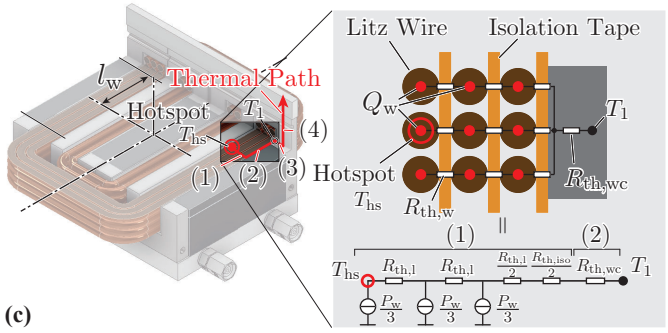
Parameters	Range
Interwinding distance	1 mm - 15 mm
Core flux density	125 mT - 350 mT
Core aspect ratio	1.5 - 3.0
Wire stranding	71 µm or 100 µm
Current density	2 $\mathrm{Amm^{-2}}$ - 6 $\mathrm{Amm^{-2}}$
Layer numbers	1 - 3
Secondary turns	4 -12



(a)



(b)



(c)

Fig. 6: Designed single-phase transformer featuring a total power of 40 kW, an efficiency of 99.68 % with 31.9 W core loss, and 94.5 W winding loss: **(a)** Geometric parameters of the transformer, yielding 17.7 µH leakage inductance. **(b)** Cooling system assembly with winding and core cooler, referred to in [29]. **(c)** The hotspot in the winding and its thermal path to the heat sink in an evenly octant-divided transformer.

$$\Delta T = P_{\rm w}\left(\frac{3R_{\rm th,l}+R_{\rm th,iso}}{2}+R_{\rm th,wc}+R_{\rm th,cc}\right), \tag{5}$$

where $R_{\rm th,l}$ represents the equivalent thermal resistance between litz wire strands layer corresponding to the considered cross-sectional area in direction (1), $R_{\rm th,iso}$ represents the thermal resistance of isolation tape in direction (1), $R_{\rm th,wc}$ represents the thermal resistance of winding cooler in direction (2), and $R_{\rm th,cc}$ represents core cooler in direction (3) and (4), respectively. As a conservative assumption, the heat transfer in the vertical direction can be neglected, i.e., the heat takes the path (1) only, $R_{\rm th,l}$ is represented as a parallel connection of $R_{\rm th,w}$ as

$$R_{\rm th,l} = R_{\rm th,w}/N_{\rm cond}, \tag{6}$$

where $R_{\rm th,w}$ represents the thermal resistance along the central axis when cylindrical conductors are placed in the radial direction with an insulating layer in between, and $N_{\rm cond}$ represents conductor number in the cross-sectional area. $P_{\rm w}$ is the total heat of the winding in the corresponding area, given as

$$P_{\rm w} = N_{\rm cond}N_{\rm layer}l_{\rm cond}Q_{\rm w}, \tag{7}$$

where $N_{\rm layer}$ represents strand layer number, $l_{\rm cond}$ represents conductor length in the cross-sectional area, and $Q_{\rm w}$ represents winding loss per length of litz wire. Note that the heat transfer due to core loss should be considered in the core cooler temperature T_1 in **Fig. 6(c)**, however, factors such as the direct contact between the core and the heat sink, relatively high thermal conductivity of the core, and the dominance of winding loss due to integrated inductor allow the temperature rise due to core loss to be neglected, similar to [29].

The thermal resistance $R_{\rm th,w}$ between litz wire with isolation tape can be derived from the model of orthogonal direction thermal resistance between cylindrical conductors with insulated layer as

$$\begin{aligned} R_{\rm th,w} &= \frac{1}{2\lambda_{\rm air}l_{\rm w}Y}, \\ Y &= \arctan\left(\sqrt{\frac{\beta+1}{\beta-1}}\right)\frac{\beta}{\sqrt{\beta^2-1}}-\frac{\pi}{4}, \\ \beta &= 1+\frac{h}{2(\lambda_{\rm iso}/\lambda_{\rm air})r}, \end{aligned} \tag{8}$$

where $\lambda_{\mathrm{air}}, \lambda_{\mathrm{iso}}$ represent the thermal conductivity of air and isolation layer, l_{w} represents a length of the conductor inside of the core, h represents a thickness of the isolation layer, and r represents a radius of the conductor [30], [31]. The thermal resistance of other parts can be derived by the following equation, determined by the geometric parameters defined by the transformer design as

$$R_{\mathrm{th,x}\in\{\mathrm{iso,wc,cc}\}} = \frac{l_{\mathrm{x}}}{\lambda_{\mathrm{x}} A_{\mathrm{x}}}, \tag{9}$$

where $l_{\mathrm{x}}, A_{\mathrm{x}}$ represents length and cross section of heat flow, and λ_{x} represents thermal conductivity of each material. The parameters of thermal conductivity and the geometric parameters of the transformer used in the estimation are shown in **Tab. V**. The temperature difference ΔT from the heat sink to the hotspot on the primary side is estimated to be 99 °C, which even satisfies the temperature index of less than 150 °C for the litz wire, when the heat sink temperature reachs 50 °C.

DC link capacitors mitigate the ripple in primary and secondary side DC bus voltages. As illustrated in **Fig. 4(b)**, all phase currents synchronize during rated operation in the four-leg inverter on the primary side, leading to a current ripple three times that of a single-phase DABC, while the ripple current on the secondary side is equivalent to a single-phase DABC. To keep the voltage ripple to values below 5 % of the primary and the secondary DC-bus, single ceramic capacitors 600 V/1 µF/X7R by Murata are parallel and series connected to reach 30 µF both on the primary and the secondary side [32].

The virtual converter prototype based on the above specifications is shown in **Fig. 7(a)**, and the simulation results at rated operation using the component data indicated above are shown in **Figs. 7(b)∼(e)**. As shown in **Fig. 7(b)**, the integrated leakage inductance allows for the realization of the DAB operation. **Fig. 7(c)** shows the current in the high-side switches of legs a and b. In the outer leg of the four-leg inverter, i.e., leg a, half the current flows compared to the inner leg b, and it can be confirmed that the current RMS values are 46.0 Arms of outer leg devices and 92.0 Arms of inner leg devices, which are 51.3 % and 54.8 % of maximum rated values of the selected switching devices. Additionally, **Fig. 7(d)** shows that a 30 µF stacked ceramic capacitor is sufficient to keep each DC-bus voltage ripple to less than 5 % of its rated voltage. Finally, **Fig. 7(e)** shows the loss breakdown of power conversion during rated operation in all phases. The switching and conduction losses are obtained using the PLECS time domain simulator with the switching device simulation model provided by each manufacturer [33]–[35], the transformer losses were calculated by the model mentioned above.

TABLE V: Thermal parameters of the cooling system.

Designator	Description	Value
Thermal conductivity		
Air	λ_{air}	$0.03\,\mathrm{W\,m^{-1}\,K^{-1}}$
Mica tape	λ_{iso}	$0.2\,\mathrm{W\,m^{-1}\,K^{-1}}$
AlSiC-9	$\lambda_{\{\mathrm{wc,cc}\}}$	$190\,\mathrm{W\,m^{-1}\,K^{-1}}$
Geometric parameters		
Litz wire	l_{w}, h, r	42.5 mm, 1 mm, 6.7 mm
Isolation layer	$l_{\mathrm{iso}}, A_{\mathrm{iso}}$	1 mm, 850 mm^2
Winding cooler	$l_{\mathrm{wc}}, A_{\mathrm{wc}}$	21.25 mm, 20 mm^2
Core cooler horizontal	$l_{\mathrm{cc1}}, A_{\mathrm{cc1}}$	5 mm, 200 mm^2
Core cooler vertical	$l_{\mathrm{cc2}}, A_{\mathrm{cc2}}$	24 mm, 100 mm^2

The results show that the power conversion efficiency, excluding the power of the cooling pump and the gate drivers and measurement and control circuits, is 98.4 %. The conduction losses in the switching device account for approximately 75 % of the total losses, and the winding and core losses in the transformer make up 20 %.

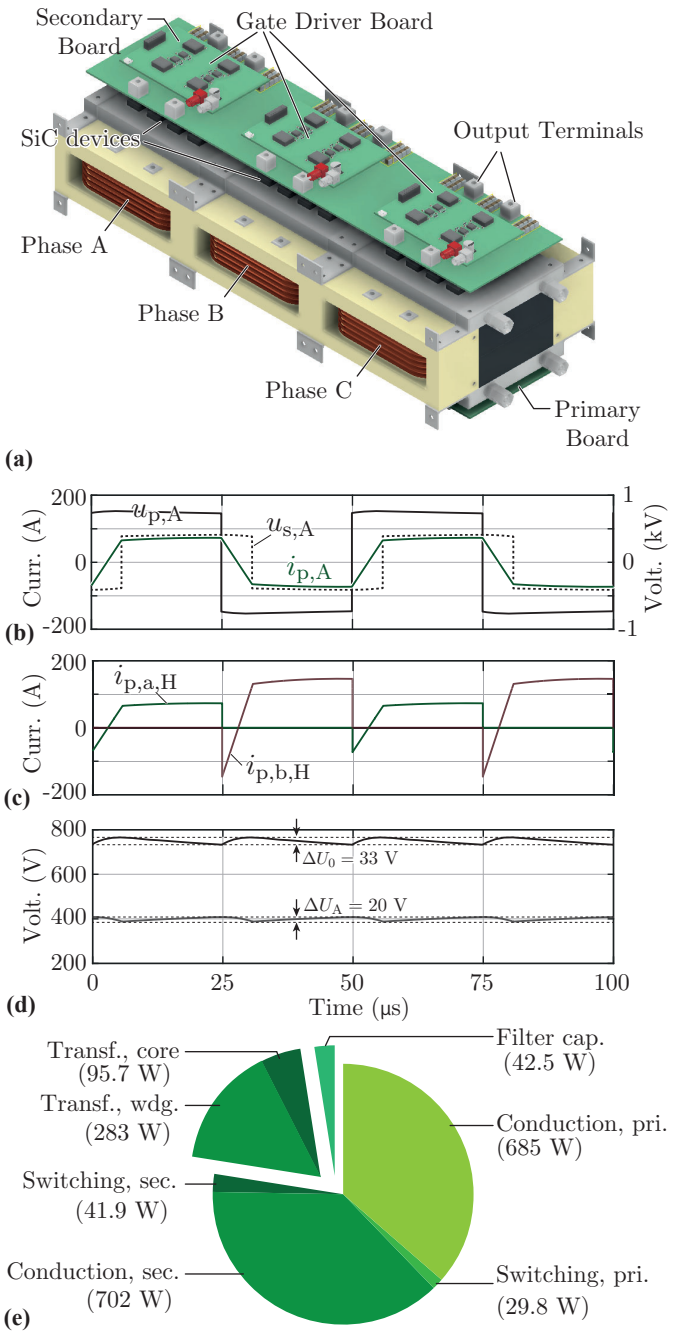


Fig. 7: Final design of the 4L3 QABC and simulation results at rated operation: **(a)** Assembly of the 4L3 QABC converter featuring boxed dimensions of 500×200×120 mm, a boxed volume of 12 dm^3, power of 3×40 kW, power density of 10 kW/dm^3, and an efficiency of 98.4 %. **(b)** Transformer current and voltage waveforms of phase A. **(c)** Switch current related to phase A, i.e., high-side switch of legs a and b. **(d)** DC bus voltage of input and output of phase A. **(e)** Total loss breakdown of the 4L3 QABC with 3×40 kW operation.

V. Conclusions

This paper introduces a novel multi-port DC/DC converter that combines three conventional dual-active bridge converters (DABC) with the primary side integrated into a single four-leg inverter, and three individually isolated output ports (4L3 quad active bridge converter, 4L3 QABC). The proposed structure reduces the number of semiconductor devices compared to the three parallel connected single-phase DABCs and offers significant advantages over a concept that employs a three-leg inverter at the primary (3L3 QABC), by fully utilizing the input voltage. The 4L3 structure demonstrated superior performance over the 3L3 QABC by consistently reducing transformer current across all operating ranges. At rated operation, the reduction of the sum of the squared transformer RMS currents reaches approximately $20\,\%$. We prove the feasibility of the 4L3 QABC by providing a virtual prototype, including the cooling system. As a result, the power conversion efficiency at a rated operation of $750\,\mathrm{V}$ primary side voltage and $400\,\mathrm{V}$ secondary side voltage at $120\,\mathrm{kW}$ is $98.4\,\%$, featuring a power density of $10\,\mathrm{kW/dm^3}$. The future work includes a hardware realization of the proposed 4L3 QABC.

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