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Comparative Evaluation of 800 V DC-Link Three-Phase Two/Three-Level SiC Inverter Concepts for Next-Generation Variable Speed Drives

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***Abstract*—The adoption of wide band-gap (WBG) semiconductors is gaining momentum, particularly in industries where high efficiency and/or extreme power density are major concerns, e.g. electric transportation and aerospace. In order to fully leverage the advantages of WBG devices, identifying the converter topologies best exploiting their superior performance is of utmost importance. Hence, this paper analyzes and compares 2-level and 3-level SiC-based three-phase inverters for next-generation variable speed drives. Full sine-wave filtering at the converter output is assumed to counteract the negative effects of the fast switching transitions of WBG devices on the driven machine. The stresses on the active and passive components, i.e. semiconductor losses, output inductor flux ripple and DC-link capacitor RMS current, are calculated by analytical and/or numerical means. Moreover, the optimal semiconductor chip area, the power losses and the efficiency of each converter topology are investigated as functions of the switching frequency, providing a theoretical performance limit for each solution. Finally, a multi-objective optimization targeting an $800\,\mathrm{V}$ $7.5\,\mathrm{kW}$ system is carried out. The results are in good agreement with the theoretical performance analysis and provide an overview of the achievable efficiency vs. power density trade-off for all the considered topologies.**

***Index Terms*—Variable Speed Drives, 2-Level Inverters, 3-Level Inverters, Wide Band-Gap Semiconductors, Semiconductor Chip Area, Multi-Objective Optimization.**

I. Introduction

Modern wide band-gap (WBG) semiconductors simultaneously enable efficiency and power density improvements in advanced power converters, as they offer unprecedented performance, leveraging on their higher switching speeds. However, fast voltage variations during switching transitions can have harmful effects in variable speed drives (VSDs), such as partial discharges in the insulating materials, i.e. motor insulation aging, voltage reflections in motor cables and bearing currents [1]. These effects can be avoided either by reducing the switching speed, or by full sine-wave filtering the inverter output voltage. While the former strategy increases the switching losses to unacceptable levels inhibiting the core advantage of WBG devices, the latter shifts the high-frequency stresses from the motor to the output filter, generally enabling an overall efficiency increase [2]. Additionally, the higher switching frequencies introduced by WBG devices limit the impact of the filter on the converter power density, and higher efficiency-to-volume figures can be achieved with respect to state-of-the-art Si-based solutions [3]. For the stated reasons, a VSD including a full sine-wave filter is considered throughout this work.

The most adopted converter topology for industrial VSDs is the three-phase (3-Φ) 2-level (2-L) inverter [1], mainly due to its simplicity and well understood operation. Nevertheless, when high DC-link voltages are required (e.g. $800\,\mathrm{V}$) the performance of this converter rapidly worsens [4], since devices with high voltage ratings are required and large high-frequency voltage harmonics are applied to the output filter, due to the 2-L nature of the switched voltage waveform. Three-level (3-L) inverter topologies represent excellent candidates to address the output filter size reduction, taking advantage of the increased number of output voltage levels [4], [5]. Moreover, employing devices with reduced voltage ratings, they ensure superior performance [6]. Even though the performance characteristics of 2-L and 3-L converters have already been investigated in literature [4], [5], [7]–[9], a comprehensive comparison between topologies taking into account the differential-mode (DM) and common-mode (CM) sine-wave filter stresses, the conduction/switching losses in the devices and the loss-optimal semiconductor chip area has yet to be addressed.

Accordingly, this paper conducts a comparative evaluation of the most suitable converter topologies for 3-Φ $800\,\mathrm{V}$ $7.5\,\mathrm{kW}$ SiC-based VSDs. This analysis considers the conventional 2-L converter (2LC) and the most widespread 3-L topologies (see **Fig. 1**), which include the T-Type converter (3LTTC), the Neutral Point Clamped converter (3LNPCC), the Active NPC converter (3LANPCC) and the Flying Capacitor converter (3LFCC). In addition, the 3-L Sparse NPC converter (3LSNPCC), introduced in [10] and analyzed in [9], [11], is considered.

The major component stresses for each topology, such as the DM and CM inductor flux ripples, the DC-link capacitor RMS current and the semiconductor losses, are calculated in **Section II**. In **Section III**, a chip area optimization procedure is proposed and applied to an $800\,\mathrm{V}$, $7.5\,\mathrm{kW}$ inverter adopting SiC MOSFETs (and SiC diodes, for the 3LNPCC). The results, expressed in terms of required filtering effort for a given efficiency target, are discussed. In **Section IV**, the efficiency vs. power density performance limits of each converter are identified by means of a multi-objective optimization procedure. Finally, a summary of the main results of this work is provided in **Section V**.

II. Component Stresses

The current and/or voltage stresses of the passive and active system components directly affect the converter design. In this section, analytical expressions are derived for all major component stresses.

A. DM and CM Inductors

The AC sine-wave filter topology illustrated in **Fig. 2**, composed of a DM and a CM filter stage, is considered herein. The most significant parameters for the design and operation of the DM and CM filter inductors are the maximum peak-to-peak and RMS flux ripple values, since the former determines the magnetic core saturation, while the latter translates in inductor winding and core losses. As the RMS flux ripple provides more information on the ripple over the complete 3-Φ output period, this is selected as the representative performance index. Assuming sufficiently large DM and CM filter capacitances (C_{DM}, C_{CM}), the RMS flux ripple in the filter inductors can be analytically derived as in [9] with the knowledge of the DM and CM inverter voltage waveforms, which depend on the converter topology and the adopted modulation strategy. Sinusoidal third-harmonic injection modulation (THIPWM) [12] is considered for the 2LC, 3LTTC, 3LNPCC, 3LANPCC (PWM-1 in [7]) and 3LFCC (as in [13]), while asymmetrical switching sequence *O* [9] is assumed for the 3LSNPCC (i.e. showing the best switching loss vs. flux-ripple trade-off). Due to the complexity of the analytically derived expressions, they are not reported herein. Nevertheless, the DM, CM and total RMS flux ripples, respectively $\Delta\Psi_{\mathrm{DM,RMS}}$, $\Delta\Psi_{\mathrm{CM,RMS}}$ and $\Delta\Psi_{\mathrm{RMS}} = \sqrt{\Delta\Psi^2_{\mathrm{DM,RMS}} + \Delta\Psi^2_{\mathrm{CM,RMS}}}$, are illustrated in normalized form (i.e. $\Delta\Psi_{\mathrm{n}} = V_{\mathrm{dc}}/f_{\mathrm{sw}}$, where f_{sw} is the converter switching frequency) in **Fig. 3**.

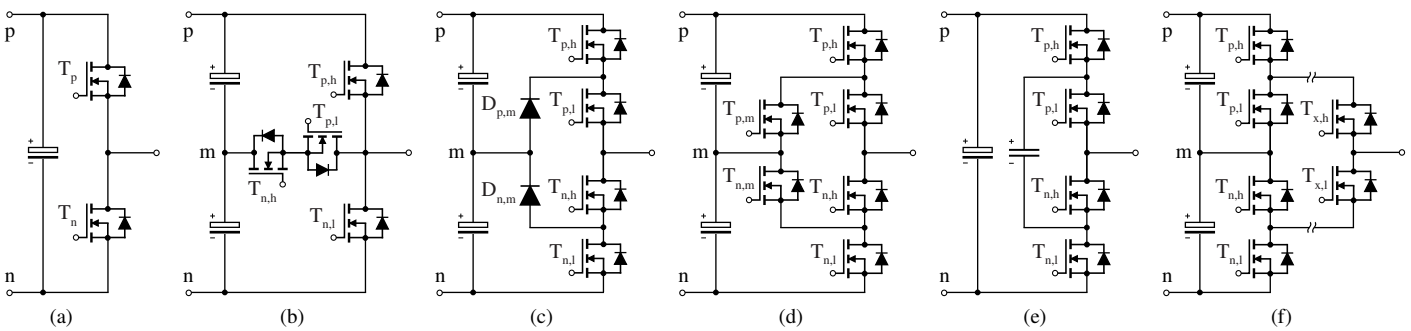

Fig. 1: Schematic of a single-phase bridge-leg of the **(a)** 2-level converter (2LC), **(b)** 3-level T-type converter (3LTTC), **(c)** 3-level neutral point clamped converter (3LNPCC), **(d)** 3-level active neutral point clamped converter (3LANPCC), **(e)** 3-level flying capacitor converter (3LFCC) and **(f)** 3-level sparse neutral point clamped converter (3LSNPCC). The 3LSNPCC bridge-leg includes the 3-L switching matrix and one 2-L inverter bridge-leg [9].

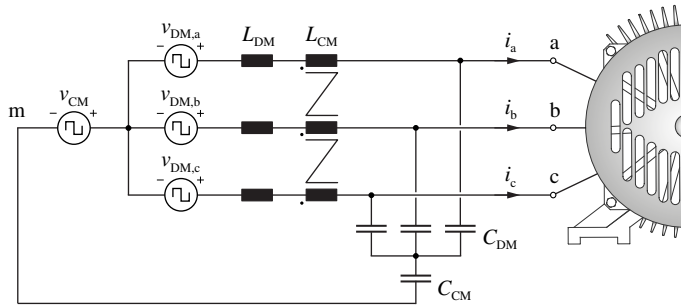

Fig. 2: Equivalent circuit of a 3-Φ inverter with the considered full sine-wave filter. The DM and CM voltages are represented by ideal switched voltage sources. Point m in the 2LC and the 3LFCC is obtained by splitting the DC-link.

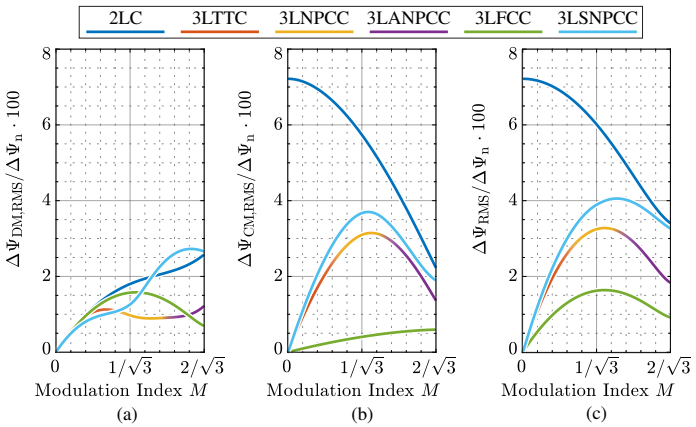

Fig. 3: Normalized RMS **(a)** DM flux ripple $\Delta\Psi_{DM,RMS}/\Delta\Psi_n$, **(b)** CM flux ripple $\Delta\Psi_{CM,RMS}/\Delta\Psi_n$ and **(c)** total flux ripple $\Delta\Psi_{RMS}/\Delta\Psi_n$, as functions of the modulation index M. The curves related to the 3LTTC, 3LNPCC and 3LANPCC are superimposed, since these converters yield the same output voltage waveform.

B. DC-Link Capacitors

Neglecting the phase current ripple, the RMS current flowing into the DC-link capacitors in balanced conditions is the same for all converters and is independent on the modulation strategy [9], [14]:

$$I_{C_{dc},RMS} = I\sqrt{M\left[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}}{\pi} - \frac{9M}{16}\right)\right]}, \quad (1)$$

where I is the phase current fundamental amplitude and φ is the load power factor angle. Nevertheless, the DC-link peak-to-peak voltage ripple generally depends on the modulation strategy itself. This effect is taken into account for the DC-link capacitor sizing in the multi-objective optimization procedure described in **Section IV**.

C. Semiconductor Devices

Conduction Losses

If MOSFETs are considered, the conduction losses have a purely resistive behavior and are proportional to the square of the conducted RMS current I_{RMS}. However, to estimate the conduction losses in the diodes of the 3LNPCC, the average current I_{AVG} is also needed. Hence, the simplified conduction loss model adopted in this work is

$$P_{cond} = V_{th}\, I_{AVG} + R\, I_{RMS}^2, \quad (2)$$

where V_{th} is the diode voltage threshold ($V_{th} = 0$ for MOSFETs) and R is the on-state (differential) resistance.

Neglecting the phase current ripple, it can be demonstrated that the RMS value of the current flowing through all MOSFETs in the 2LC and the 3LFCC is independent on the modulation strategy and equals $I/2$. Nevertheless, the remaining 3-L converters yield more complicated expressions. If THIPWM is considered for the 3LTTC, 3LNPCC and 3LANPCC,

$$I_{p,RMS} = I_{n,RMS} = I\sqrt{M\left(\frac{37}{90\pi} + \frac{7}{30\pi}\cos^2\varphi\right)}, \quad (3)$$

$$I_{m,RMS} = I\sqrt{\frac{1}{2} - M\left(\frac{37}{45\pi} + \frac{7}{15\pi}\cos^2\varphi\right)}, \quad (4)$$

$$I_{m,AVG} = \frac{IM}{2}\left[\cos\varphi\left(\frac{2|\varphi|}{\pi} + \frac{\cos\varphi\sin|\varphi|}{3\pi} - 1\right) - \frac{7\sin|\varphi|}{3\pi} + \frac{4}{\pi}\right], \quad (5)$$

TABLE I: Average and RMS current stress expressions for the semiconductor devices of all the considered converter topologies.

Topology	Device	I_{AVG}	I_{RMS}
2LC	T_p, T_n	–	$I/2$
3LTTC	$T_{p,h}$, $T_{n,l}$	–	$I_{p,RMS} = I_{n,RMS}$
	$T_{p,l}$, $T_{n,h}$	–	$I_{m,RMS}$
3LNPCC	$T_{p,h}$, $T_{n,l}$	–	$I_{p,RMS} = I_{n,RMS}$
	$T_{p,l}$, $T_{n,h}$	–	$I/2$
	$D_{p,m}$, $D_{n,m}$	$I_{m,AVG}/2$	$I_{m,RMS}/\sqrt{2}$
3LANPCC	$T_{p,h}$, $T_{n,l}$	–	$I_{p,RMS} = I_{n,RMS}$
	$T_{p,l}$, $T_{n,h}$	–	$I/2$
	$T_{p,m}$, $T_{n,m}$	–	$I_{m,RMS}/\sqrt{2}$
3LFCC	$T_{p,h}$, $T_{n,l}$, $T_{p,l}$, $T_{n,h}$	–	$I/2$
3LSNPCC	$T_{x,h}$, $T_{x,l}$	–	$I/2$
	$T_{p,h}$, $T_{n,l}$	–	$I_{T_{p,h},RMS}$
	$T_{p,l}$, $T_{n,h}$	–	$I_{T_{p,l},RMS}$

where subscripts p, n and m refer to the currents flowing in the positive, negative and middle DC-link rails, respectively, can be conveniently derived. In fact, (3), (4) and (5) are sufficient to completely identify the current stresses in all semiconductor devices, as reported in **Table I**. Finally, the RMS current expressions for the transistors of the 3LSNPCC are $I_{T_{x,h},RMS} = I_{T_{x,l},RMS} = I/2$ for the 2-L inverter devices and

$$I_{T_{p,h},RMS} = I_{T_{n,l},RMS} = I\sqrt{\frac{\sqrt{3}}{4\pi}M(4\cos^2\varphi + 1)}, \quad (6)$$

$$I_{T_{p,l},RMS} = I_{T_{n,h},RMS} = \begin{cases} I\sqrt{\frac{1}{2} - \frac{\sqrt{3}}{8\pi}\left[6M + \cos(2\varphi)\,(M-3)\right]} & \text{Area } ① \\ I\sqrt{\frac{1}{2} - \frac{\sqrt{3}}{4\pi}\left[3M - \cos(2\varphi)\,(\sqrt{3}\pi - 3 - 2M)\right]} & \text{Area } ② \end{cases}, \quad (7)$$

for the 3-L switching matrix devices, where area ① and area ② are defined in [11].

Switching Losses

The switching losses of a generic MOSFET half-bridge can be expressed as [15]

$$E_{sw} = Q_{oss}(V_{sw})\, V_{sw} + Q_{rr}(i_{sw})\, V_{sw} + \frac{1}{2}\frac{V_{sw}^2}{dv/dt}\, i_{sw} + \frac{1}{2}\frac{V_{sw}}{di/dt}\, i_{sw}^2, \quad (8)$$

where V_{sw} and i_{sw} are the switched voltage and current, respectively, Q_{oss} is the charge stored in the semiconductor device non-linear output capacitance and Q_{rr} is the reverse-recovery charge of the MOSFET body-diode. The last two terms of (8) represent the v-i overlap losses and depend on the voltage and current time derivatives during the overlap time. Soft-switching transitions, i.e. with $i_{sw} < 0$, are typically considered lossless.

Assuming infinitely fast transitions, the v-i overlap loss contributions can be neglected and the Q_{rr} becomes equal to the forward-bias injected charge [16], i.e. $Q_{rr} \approx \tau\, i_{sw}$, where τ is the charge carrier recombination lifetime.This approximation results in a linear switching loss model with respect to the switched current, obtaining

$$E_{sw}(i_{sw}) \approx Q_{oss}(V_{sw})\, V_{sw} + \tau\, V_{sw}\, i_{sw} = k_0 + k_1\, i_{sw}, \quad (9)$$

which represents a theoretical lower limit for the switching losses and is in a first approximation met in practice for semiconductor devices with high switching performance [6].

Equations (8) and (9) quantify the hard switching losses generated in a conventional half-bridge with identical high-side and low-side semiconductor devices. However, these expressions can be extended to other bridge-leg topologies by analyzing the capacitive and reverse-recovery charges involved in each commutation process, depending on the topology being considered and on the different devices involved in the transition. To facilitate this, the equivalent circuit of a 3-L bridge-leg illustrated in **Fig. 4** is considered. In general, a total of four different switching events can occur, depending on the direction of the switch-

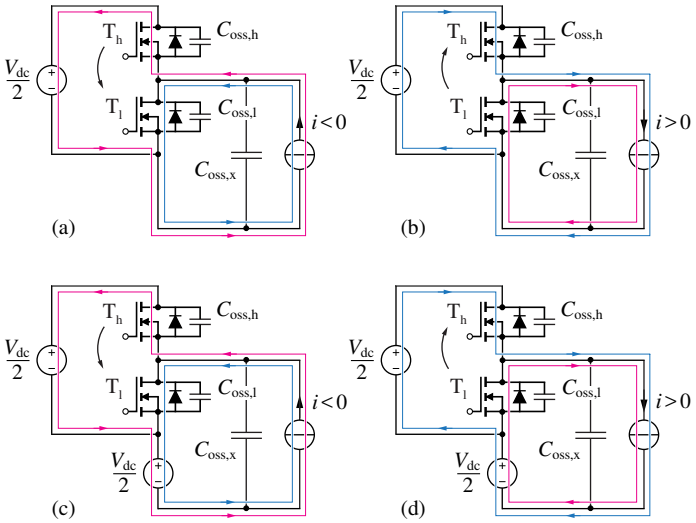

Fig. 4: Equivalent circuits of a generic 3-L bridge-leg involved in the four possible hard-switching events: the current paths before and after the transition are highlighted in pink and blue, respectively. $C_{oss,x}$ represents the output capacitance of a generic device subject to voltage variation but not directly involved in the commutation.

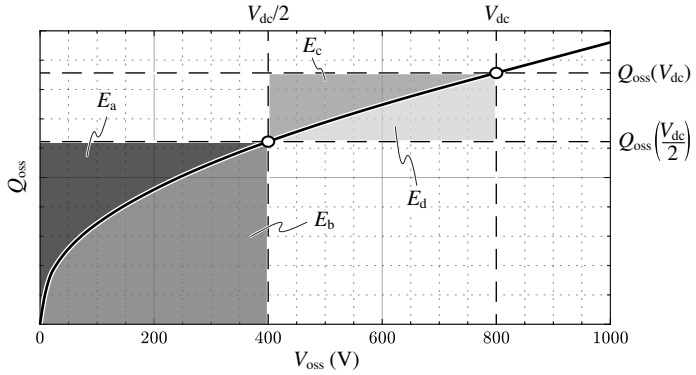

Fig. 5: Graphical representation of the capacitive energy components E_a, E_b, E_c and E_d of a generic semiconductor device in a 3-L inverter with $V_{dc} = 800\,\text{V}$.

node current i and the magnitude of the offset voltage applied to the switch-node capacitance $C_{oss,x}$. Transistors T_h and T_l represent the two switches directly involved in the commutation process, while $C_{oss,x}$ represents the output capacitance of a generic device which is subject to the voltage variation. All four switching events (a), (b), (c) and (d) are analyzed under the hypothesis of instantaneous transitions (i.e. no v-i overlap losses), exploiting the energy balance method reported in [17]. For reasons of conciseness, the following energy terms are defined:

$$E_a = E_{oss}(V_{dc}/2), \tag{10}$$

$$E_b = Q_{oss}(V_{dc}/2)\frac{V_{dc}}{2} - E_{oss}(V_{dc}/2), \tag{11}$$

$$E_c = [E_{oss}(V_{dc}) - E_{oss}(V_{dc}/2)] - [Q_{oss}(V_{dc}) - Q_{oss}(V_{dc}/2)]\frac{V_{dc}}{2}, \tag{12}$$

$$E_d = [Q_{oss}(V_{dc}) - Q_{oss}(V_{dc}/2)]V_{dc} - [E_{oss}(V_{dc}) - E_{oss}(V_{dc}/2)], \tag{13}$$

where Q_{oss} and E_{oss} refer respectively to the charge and the energy stored in the generic capacitance C_{oss}. These expressions are graphically illustrated in **Fig. 5** for $V_{dc} = 800\,\text{V}$. Leveraging (10)-(13), the capacitive losses for the four switching events are

$$E_{loss,(a)} = E_{b,h} + E_{a,l} + E_{a,x}, \tag{14}$$

$$E_{loss,(b)} = E_{a,h} + E_{b,l} + E_{b,x}, \tag{15}$$

$$E_{loss,(c)} = E_{b,h} + E_{a,l} + E_{c,x}, \tag{16}$$

$$E_{loss,(d)} = E_{a,h} + E_{b,l} + E_{d,x}, \tag{17}$$

where subscripts h, l and x refer to $C_{oss,h}$, $C_{oss,l}$ and $C_{oss,x}$, respectively. For instance, the hard switching commutation in (a) and (c) is the same, however a $V_{dc}/2$ output DC-bias is present in the latter case. When T_h turns off, i transitions from the MOSFET channel to its body diode, until T_l is turned on. Once this occurs, the capacitive energy stored in $C_{oss,l}$ is dissipated ($E_{a,l}$) and part of the energy provided by the DC-link to charge $C_{oss,h}$ is lost in the circuit resistances ($E_{b,h}$). The output capacitance $C_{oss,x}$ is practically in parallel with T_l, however it is subject

TABLE II: Overview of the capacitive losses for all the considered topologies. Where possible, the symmetry between upper and lower half of the bridge-leg is exploited (i.e. the results are the same and thus not reported). Moreover, the semiconductor devices subject to equal current and switching stresses during a 3-Φ output period are considered to be equal, e.g. $T_p = T_n$ for the 2LC, $T_{p,h} = T_{p,l} = T_{n,h} = T_{n,l}$ for the 3LFCC, etc. (cf. **Table I**). The hard-switching events are defined by the direction of the current flowing out of the equivalent switch-node involved in the transition (i.e. i, cf. **Fig. 4**).

Topology	Transition	Capacitive Losses
2LC	$T_p \leftarrow T_n\ (i>0)$ $T_p \rightarrow T_n\ (i<0)$	$Q_{oss,T_p}(V_{dc})V_{dc}$
3LTTC	$T_{p,h} \leftarrow T_{p,l}\ (i>0)$	$E_{a,T_{p,h}} + E_{b,T_{p,l}} + E_{d,T_{n,l}}$
	$T_{p,h} \rightarrow T_{p,l}\ (i<0)$	$E_{b,T_{p,h}} + E_{a,T_{p,l}} + E_{c,T_{n,l}}$
3LNPCC	$T_{p,h} \leftarrow T_{n,h}\ (i>0)$	$E_{a,T_{p,h}} + E_{b,T_{n,h}} + E_{b,D_{p,m}}$
	$T_{p,h} \rightarrow T_{n,h}\ (i<0)$	$E_{b,T_{p,h}} + E_{a,T_{n,h}} + E_{a,D_{p,m}}$
3LANPCC	$T_{p,h} \leftarrow T_{p,m}\ (i>0)$	$E_{a,T_{p,h}} + E_{b,T_{n,h}} + E_{b,T_{p,m}}$
	$T_{p,h} \rightarrow T_{p,m}\ (i<0)$	$E_{b,T_{p,h}} + E_{a,T_{n,h}} + E_{a,T_{p,m}}$
3LFCC	$T_{p,h} \leftarrow T_{n,l}\ (i>0)$ $T_{p,h} \rightarrow T_{n,l}\ (i<0)$ $T_{p,l} \leftarrow T_{n,h}\ (i>0)$ $T_{p,l} \rightarrow T_{n,h}\ (i<0)$	$Q_{oss,T_{p,h}}(V_{dc}/2)V_{dc}/2$
3LSNPCC	$T_{x,h} \leftarrow T_{x,l}\ (i>0)$ $T_{x,h} \rightarrow T_{x,l}\ (i<0)$	$Q_{oss,T_{x,h}}(V_{sw})V_{sw}$*
	$T_{p,h} \leftarrow T_{p,l}\ (i>0,\ T_{n,h}\ \text{on})$	$E_{a,T_{p,h}} + E_{b,T_{p,l}} + 3E_{b,T_{x,h}}$
	$T_{p,h} \rightarrow T_{p,l}\ (i<0,\ T_{n,h}\ \text{on})$	$E_{b,T_{p,h}} + E_{a,T_{p,l}} + 3E_{a,T_{x,h}}$
	$T_{p,h} \leftarrow T_{p,l}\ (i>0,\ T_{n,l}\ \text{on})$	$E_{a,T_{p,h}} + E_{b,T_{p,l}} + 3E_{d,T_{x,h}}$
	$T_{p,h} \rightarrow T_{p,l}\ (i<0,\ T_{n,l}\ \text{on})$	$E_{b,T_{p,h}} + E_{a,T_{p,l}} + 3E_{c,T_{x,h}}$

* $V_{sw} = \{0,\ V_{dc}/2,\ V_{dc}\}$ depending on the 3-L switching matrix state [9].

TABLE III: Nominal operating conditions of the considered VSD system.

Parameter	Description	Value
V_{dc}	DC-link voltage	800 V
M	modulation index	0.85
V	peak output phase voltage	340 V
I	peak output phase current	14.7 A
$\cos\varphi$	power factor	1
P	output power	7.5 kW
f	output frequency	0 . . . 300 Hz

to different voltage transitions in the two situations, dissipating $E_{a,x}$ in (a) ($V_{dc}/2 \rightarrow 0$) and $E_{c,x}$ in (c) ($V_{dc} \rightarrow V_{dc}/2$). Therefore, applying these considerations to each topology and analyzing all different switching transition, the results reported in **Table II** are obtained.

III. Optimal Chip Area

In this section, the loss-optimal semiconductor chip area for each topology is calculated, in order to identify a theoretical upper limit to the efficiency performance of each solution. The component losses are calculated based on simplified analytical models given in **Section II**. This analysis is applied to an 800 V 7.5 kW VSD, assuming the nominal operating conditions reported in **Table III** and market available semiconductor devices.

A. Semiconductor Statistical Analysis

First, the relevant performance characteristics of the considered semiconductor devices must be identified. For the sake of the present analysis, the 3rd generation SiC MOSFETs and the 5th generation SiC diodes from Wolfspeed [18] are selected, mainly due to the availability of semiconductor chip size information from the manufacturer and in-house switching loss measurements.

The most important performance indicator for high-voltage power MOSFETs is the $R_{DS}\,Q_{oss}$ product [19], which provides a first insight of the achievable conduction and switching performance. A $Q_{oss}(R_{DS})$ fitting procedure, assuming $Q_{oss} \propto 1/R_{DS}$, is carried out for the selected 650 V and 1200 V MOSFETs and is reported in **Fig. 6**. Additionally,

TABLE IV: Parameters of the considered SiC MOSFETs and SiC Schottky diodes from Wolfspeed [18] (at $T_j = 25\,^\circ\mathrm{C}$). All parameters which depend on the semiconductor chip area A are reported in normalized form, i.e. $r = R\,A$, $q_{oss} = Q_{oss}/A$ and $e_x = E_x/A$.

Device	V_{th}	r	q_{oss}*	e_a	e_b	e_c	e_d	τ
1200 V MOSFET	–	$410\,\mathrm{m\Omega\,mm^2}$	$14.2\,\mathrm{nC/mm^2}$	$1.28\,\mathrm{\mu J/mm^2}$	$2.78\,\mathrm{\mu J/mm^2}$	$0.79\,\mathrm{\mu J/mm^2}$	$0.85\,\mathrm{\mu J/mm^2}$	6.82 ns
650 V MOSFET	–	$295\,\mathrm{m\Omega\,mm^2}$	$11.6\,\mathrm{nC/mm^2}$	$1.54\,\mathrm{\mu J/mm^2}$	$3.10\,\mathrm{\mu J/mm^2}$	–	–	5.95 ns
650 V diode	0.96 V	$96.0\,\mathrm{m\Omega\,mm^2}$	$12.5\,\mathrm{nC/mm^2}$	$1.89\,\mathrm{\mu J/mm^2}$	$3.09\,\mathrm{\mu J/mm^2}$	–	–	–

*evaluated at 800 V for 1200 V devices and at 400 V for 650 V devices.

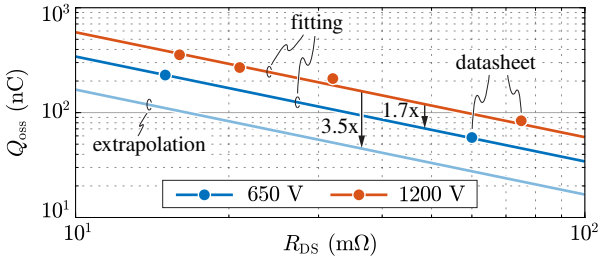

Fig. 6: Output capacitance charge Q_{oss} dependence on the drain-source resistance R_{DS} for the considered 650 V ($V_{DS} = 400$ V) and 1200 V ($V_{DS} = 800$ V) SiC MOSFETs from Wolfspeed [18]. The fitting curves assuming $Q_{oss} \propto 1/R_{DS}$ are shown with straight lines. The 650 V characteristic obtained from analytical extrapolation of the performance of 1200 V devices according to traditional scaling laws [19] is illustrated for reference purposes, highlighting the significantly worse performance of real 650 V devices.

the fitted characteristic for 650 V MOSFETs is compared to a theoretical extrapolation from 1200 V devices, considering traditional scaling laws [19], highlighting that the real performance of the lower-voltage devices is quite far from theoretical expectations. This is mainly due to the MOSFET epitaxial layer resistance becoming less dominant with respect to other resistance components at low breakdown voltages [20], hence causing the total on-state resistance not to scale as expected. Therefore, since the performance ratio between 650 V and 1200 V devices plays a major role in defining the relative comparison between converter topologies, the ones adopting lower-voltage devices are expected to perform worse than expected from previous analyses [19].

The conduction characteristics of MOSFETs and diodes, according to (2), are derived from a fitting of the information provided in the datasheets, obtaining the voltage threshold V_{th} (for diodes) and the differential on-state resistance per-unit of chip area r. A similar fitting procedure is performed for the charge and energy stored in the semiconductor device non-linear output capacitance, which scale proportionally to the device chip area A, and for the reverse-recovery time constant τ, which is independent on A. All the parameters that depend on A are reported in **Table IV** in normalized form, i.e. with a lower-case letter. Moreover, a linear dependence on the semiconductor junction temperature T_j is assumed for all the temperature dependent parameters (i.e. V_{th}, r and τ), expressed by

$$X(T_j) = [1 + \alpha_X\,(T_j - 25)]\,X(25\,^\circ\mathrm{C}), \tag{18}$$

where X is the parameter under consideration, T_j is expressed in °C and α_X is a coefficient obtained from fitting (see **Table V**).

B. Chip Area Optimization

The proposed chip area optimization procedure aims to identify the combination of semiconductor chip sizes inside a bridge-leg that minimizes the overall converter losses, meanwhile complying with the maximum operating T_j of each device. Since the conduction losses decrease with increasing A (i.e. $R \propto 1/A$), while the switching losses tend to increase (i.e. $Q_{oss} \propto A$, $E_x \propto A$), a performance trade-off is clearly present and an overall loss-optimal chip area can be found [19].

To quantitatively determine the optimal A, accurate semiconductor loss and thermal models need to be defined. The conduction losses in each semiconductor device are obtained according to (2), leveraging the average and RMS current expressions reported in **Table I**. Moreover, the approximated switching loss model presented in **Section II**, i.e. neglecting the v-i overlap losses and considering only the unavoidable charge-related loss contributions, is adopted herein, as it relies purely on the manufacturer's datasheet information. In particular, this model allows to determine the highest theoretical efficiency of each analyzed topology, hence providing an upper limit to the converter performance, independent on the practical circuit layout. Since the chip size of a semiconductor device can influence the switching losses of other devices, the loss distribution among the bridge-leg devices is analyzed for each transition of **Table II**. The reverse-recovery charge is assumed to be dissipated inside the transistor that is turning on, while some

TABLE V: Thermal dependence coefficients of the considered SiC MOSFETs and SiC Schottky diodes from Wolfspeed [18].

Device	$\alpha_{V_{th}}$ ($^\circ\mathrm{C}^{-1}$)	α_r ($^\circ\mathrm{C}^{-1}$)	α_τ ($^\circ\mathrm{C}^{-1}$)
1200 V MOSFET	–	4.7×10^{-3}	8.0×10^{-3}
650 V MOSFET	–	2.1×10^{-3}	4.9×10^{-3}
650 V diode	-1.5×10^{-3}	6.4×10^{-3}	–

capacitive energy components are lost in the hard-switching transistor and others are distributed between the conducting transistors/diodes in the commutation loop, according to their on-state resistance. Therefore, by fixing the topology, the modulation strategy, the semiconductor chip areas and the operating f_{sw}, the total semiconductor losses P_{tot} of each device can be calculated.

To estimate T_j, the junction-to-heatsink thermal resistance expression

$$R_{th,[K/W]} = 23.94\,A_{[mm^2]}^{-0.88}, \tag{19}$$

proposed in [21] is adopted herein. This expression accounts for the heat spreading taking place between the chip and the heatsink. Each semiconductor junction temperature can thus be calculated as

$$T_j = T_{hs} + R_{th}\,P_{tot}, \tag{20}$$

where $T_{hs} = 80\,^\circ\mathrm{C}$ is the heatsink temperature.

Leveraging the described chip area dependent loss and thermal models, together with the semiconductor parameters reported in **Table IV** and **Table V**, a converter chip size optimization is performed. A large number of chip size combinations are analyzed, deriving the electrical resistance and the capacitive charge/energy components of the semiconductors from their specific values and calculating the chip thermal resistance according to (19). Both T_j and P_{tot} are obtained by iterative means, considering nominal operation. Therefore, the converter designs with at least one device exceeding the maximum junction temperature limit of 175 °C are discarded, while the admissible design that minimizes the total converter losses is selected.

C. Performance Comparison

The chip area optimization algorithm is run for the nominal operating point (cf. **Table III**) and $f_{sw} = 5 \ldots 500$ kHz. The results are illustrated in **Fig. 7**, where the semiconductor efficiency η_{semi} and the output total RMS flux ripple $\Delta\Psi_{RMS}$ are shown for each topology. To carry out a practical performance comparison between the analyzed solutions, a target $\eta_{semi} = 99.5\,\%$ is considered. The necessary operating f_{sw} to achieve the desired η_{semi} for each converter topology is derived as illustrated in **Fig. 7(a)**, yielding different $\Delta\Psi_{RMS}$ values at the converter output as shown in **Fig. 7(b)**. In particular, $\Delta\Psi_{RMS}$ can be considered a qualitative performance indicator of the output filter size and/or loss, thus enabling a straightforward preliminary performance comparison among topologies. The results of this analysis are reported in **Table VI**.

The best performance is achieved by the 3LTTC, which ensures the minimum overall $\Delta\Psi_{RMS}$ and also the minimum semiconductor chip area A_S among 3-L topologies. On the other hand, the 2LC shows the worst output $\Delta\Psi_{RMS}$, as already expected from previous analyses [4], [5], [9]. The 3LTTC is particularly favored by its low number of semiconductor devices and by the similar performance characteristics of 650 V and 1200 V MOSFETs (cf. **Fig. 6** and **Table IV**), which enable switching performance comparable to other 3-L topologies. The 3LNPCC and the 3LANPCC coincidentally yield the same results for $\eta_{semi} = 99.5\,\%$, however they perform differently if other efficiency targets are assumed. In particular, the 3LNPCC shows the worst overall performance at low f_{sw} (i.e. high η_{semi} target). This behavior is determined by the SiC Schottky diodes, which feature a substantial current-independent voltage drop (i.e. V_{th}) and set an upper limit to the converter efficiency. Nevertheless they are characterized by no reverse-recovery losses and low capacitively stored charge (i.e. due to their small chip size), thus outperforming all other solutions at high f_{sw}. Even though the 3LFCC seems comparable to the 2LC from an efficiency perspective, its frequency doubling characteristic yields

TABLE VI: Switching frequency f_{sw}, total semiconductor chip area A_S and total RMS flux ripple $\Delta\Psi_{RMS}$ comparison among the analyzed topologies, designed for nominal operation (cf. **Table III**) and assuming a semiconductor efficiency target $\eta_{semi} = 99.5\,\%$ (i.e. $P_{semi} = 37.5\,\mathrm{W}$).

Parameter	Description	2LC	3LTTC	3LNPCC	3LANPCC	3LFCC	3LSNPCC
f_{sw}	switching frequency	36 kHz	84 kHz	59 kHz	59 kHz	40 kHz	61 kHz
A_S	total semiconductor chip area	75.9 mm^2	146 mm^2	213 mm^2	231 mm^2	166 mm^2	186 mm^2
$\Delta\Psi_{RMS}$	total RMS flux ripple	1.05 V ms	0.28 V ms	0.40 V ms	0.40 V ms	0.30 V ms	0.53 V ms

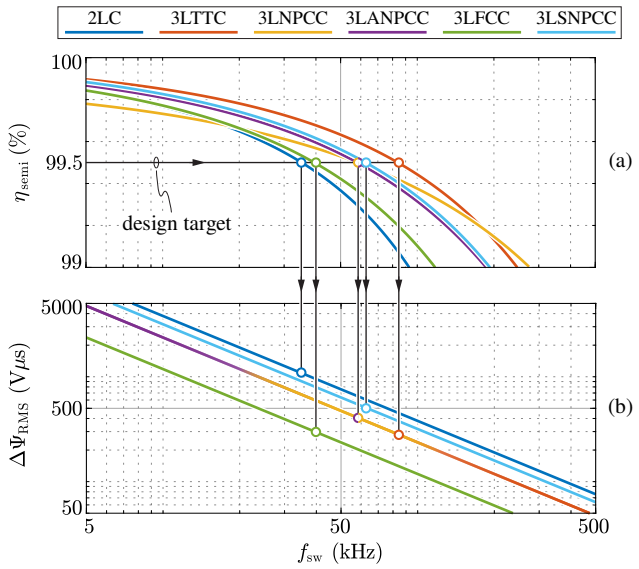

Fig. 7: Results of the chip area optimization for the analyzed topologies in nominal operating conditions (cf. **Table III**), considering the chip thermal dissipation limits. **(a)** semiconductor efficiency η_{semi} and **(b)** total output RMS flux ripple $\Delta\Psi_{RMS}$ as functions of the converter switching frequency f_{sw}. A semiconductor efficiency of 99.5 % is targeted, hence an operating f_{sw} for each converter topology is derived in **(a)** and, consequently, $\Delta\Psi_{RMS}$ is obtained in **(b)**, providing a direct performance comparison among the different solutions (cf. **Table VI**). The results for the 3LNPCC and the 3LANPCC are coincidentally the same for $\eta_{semi} = 99.5\,\%$ and are thus superimposed.

the lowest $\Delta\Psi_{RMS}$ (cf. **Fig. 3(c)**), therefore its overall performance results comparable to the one of the 3LTTC. Finally, the 3LSNPCC is positioned as the last of the 3-L topologies, mainly due to the large capacitive losses involved in the commutation transitions of the 3-L switching matrix (cf. **Table II**) and a higher output $\Delta\Psi_{RMS}$ with respect to conventional 3-L converters (cf. **Fig. 3(c)**).

IV. Multi-Objective Optimization

This section describes the design and optimization of a 3-Φ 7.5 kW inverter for VSD applications, with the specifications reported in **Table III**. A multi-objective optimization is carried out for all the analyzed topologies, such that a complete performance comparison between the solutions is obtained. First, the design variables and constraints forming the converter *design space* are selected and the considered volume and loss models of the system components are described. Then, the optimal converter designs with respect to efficiency (η) and volumetric power density (ρ) are identified by means of a Pareto analysis in the *performance space*.

A. Design Space

The operating switching frequency f_{sw} of the converter is varied among 10, 20, ..., 200 kHz. The DC-link capacitance is calculated to obtain a 1 % peak-to-peak voltage ripple with respect to V_{dc}, where additional capacitance needed for energy storage or motor braking overvoltage requirements is neglected in this analysis. The output DM/CM sine-wave filter is designed to achieve the smallest possible size, setting both filter corner frequencies $f_{c,DM}$ and $f_{c,CM}$ to the maximum value that does not interfere with the switching harmonics (here considered to be $f_{sw}/4$). Several DM inductance values L_{DM} are spaced logarithmically between a minimum and a maximum values, in order to avoid excessive peak-to-peak current ripple (100 % of I) and unacceptable voltage drop (10 % of V). The DM capacitance is calculated consequently from $f_{c,DM}$ and L_{DM}, where all the designs exceeding 25 % reactive current in the DM capacitor are discarded. The CM filter inductance L_{CM} is selected such that the CM RMS current ripple is equal to 5 % of I. In this way, the effect of this additional high-frequency current contribution on DM inductors and power devices can be disregarded, reducing the number of design combinations. The CM capacitance is thus derived from $f_{c,CM}$ and L_{CM}.

Once all combinations of the sine-wave filter parameters are defined, the output voltage and current waveforms are generated, so that the semiconductor losses can be calculated and the magnetic components can be designed. The 3rd generation SiC MOSFETs (650 V, 1200 V) and 5th generation SiC diodes (650 V) from CREE [18] are considered in this analysis, assuming the possibility to parallel up to 4 devices. The semiconductor loss calculation is based on the conduction and switching loss models described in **Section II**, which depend on the device junction temperature T_j by means of V_{th}, R and Q_{rr}. In particular, the complete switching loss model taking into account the v-i overlap losses is considered. The values of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ are derived from the measured loss data of the C3M0032120K SiC MOSFET and are scaled for other transistors according to their chip area A ($\mathrm{d}v/\mathrm{d}t \approx \mathrm{cost}$, $\mathrm{d}i/\mathrm{d}t \propto A$) [22], while the charge related loss parameters are obtained from the manufacturer's datasheets. The semiconductor junction-to-ambient thermal model assumes the junction-to-case thermal resistance provided by the manufacturer, a case-to-heatsink contribution of 1.0 K/W derived from available hardware prototypes adopting a TO-247 package, and a constant heatsink temperature of $T_{hs} = 80\,^{\circ}\mathrm{C}$. Leveraging the introduced temperature dependent semiconductor loss models and the junction-to-heatsink thermal model, the operating junction temperature of each device is iteratively calculated and those designs that include at least one device with $T_j > 175\,^{\circ}\mathrm{C}$ are discarded. Moreover, the total converter semiconductor losses allow to size the heatsink exploiting the CSPI method [23], considering $\mathrm{CSPI} = 15\,\mathrm{W/K\,dm^3}$ and $\Delta T = 50\,^{\circ}\mathrm{C}$ (i.e. 30 °C ambient temperature). The DM and CM inductors are accurately designed and optimized with the tool presented in [24], which provides estimated volume and losses of all the thermally-feasible designs. All DC-side and AC-side capacitors are selected within the most compact (ceramic) solutions available on the market. The volume of PCBs (power and gate drivers) and the power consumption of auxiliary circuits (control and measurement) are estimated from available hardware prototypes. Finally, a 20 % total volume increase is assumed, accounting for practical realization.

B. Performance Space

The results of the optimization procedure for each topology are shown in the η-ρ performance plane in **Fig. 8**, where the Pareto-optimal designs are identified and highlighted.

In general, it is observed that the maximum achievable converter efficiency values are lower than in **Section III**, since the multi-objective optimization takes into account the v-i overlap switching losses, the winding and core losses in the sine-wave filter inductors and the power consumed by the auxiliary components, e.g. gate drivers and control. Nevertheless, the results confirm and substantiate the relative comparison between topologies reported in **Fig. 7**.

As expected, the best performing candidate (i.e. showing the largest Pareto envelope in **Fig. 9**) is the 3LTTC, closely followed by the 3LFCC. In particular, the 3LTTC can be designed for a volumetric power density of 37.8 kW/dm³ while still achieving an efficiency of 99.0 %, including the sine-wave filter. The Pareto-optimal operating switching frequencies for all converters vary in the range of 10...80 kHz, being the lowest for the 3LFCC, due to its frequency-doubling characteristic at the output. For higher switching frequencies the increase in switching losses leads to a larger heatsink, which more than offsets the volume reduction of the sine-wave filter components and thus leads to both lower efficiency and higher total volume. The solutions showing the worst overall performance are the 2LC, as anticipated by previous literature [4], [5], and interestingly the 3LNPCC. Even though the 2LC is evidently limited in efficiency, due to switching losses, and in power density, due to the 2-L output voltage waveform resulting in a larger filter, the excellent performance of 1200 V SiC MOSFETs reduces the expected gap with respect to 3-L topologies. On the other hand, the non-ideal performance of 650 V MOSFETs (cf. **Section III**) and the significant diode current-independent voltage drop are the main responsibles of the performance shortcomings of the 3LNPCC. In particular, when aiming for high

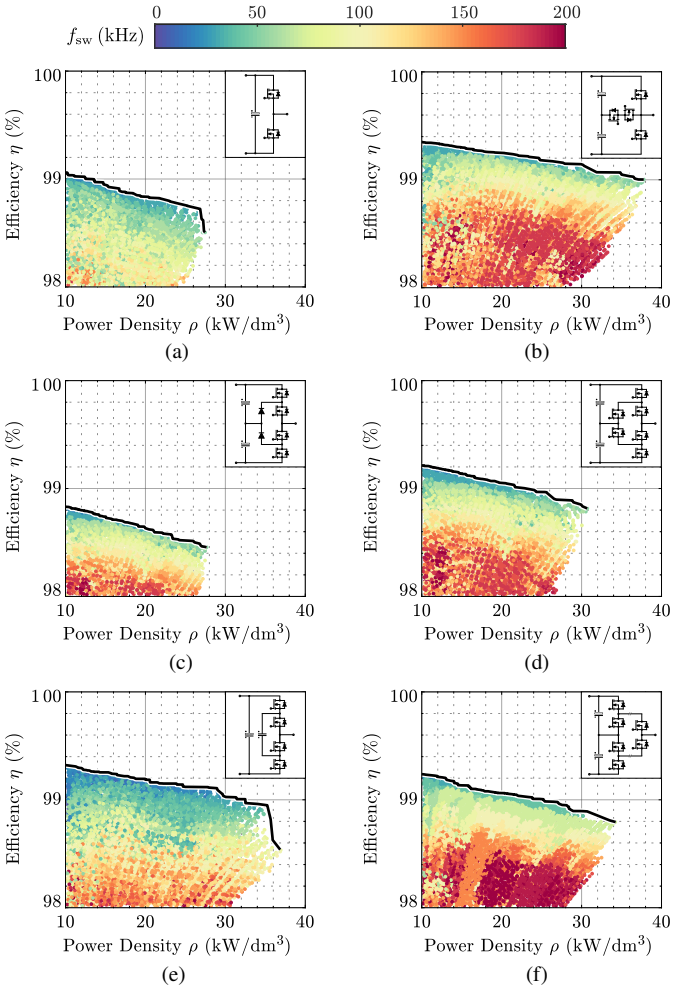

Fig. 8: Results of the converter optimization procedure in the efficiency vs. volumetric power density (η-ρ) performance plane, considering nominal operating conditions (cf. **Table III**). **(a)** 2LC, **(b)** 3LTTC, **(c)** 3LNPCC, **(d)** 3LANPCC, **(e)** 3LFCC and **(f)** 3LSNPCC. Each dot represents a single converter design, while the solid black lines indicate the Pareto fronts.

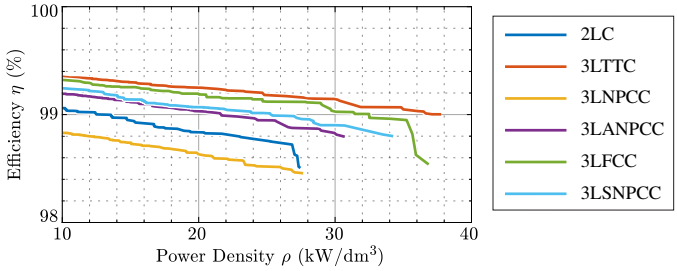

Fig. 9: Overview of the Pareto fronts of all topologies in the η-ρ plane.

efficiency design targets, the diode conduction losses yield a negative performance offset (i.e. compared with the 3LANPCC in **Fig. 8(d)**) which cannot be compensated by the switching loss reduction in the considered f_{sw} range. Moreover, the higher resulting semiconductor losses translate in a larger heatsink requirement, thus affecting also the converter power density. Additionally, for the considered 7.5 kW application the semiconductor device packages (i.e. TO-247) and their allocated PCB space significantly affect the converter volume, therefore topologies with high component count are penalized. The 3LANPCC counteracts the 3LNPCC drawbacks related to the adoption of SiC diodes, by replacing them with 650 V MOSFETs. Nevertheless, it does not achieve performance comparable to the 3LTTC or the 3LFCC, mostly due to its higher semiconductor device count. Finally, unexpected from the theoretical analysis of **Section III**, the 3LSNPCC performs slightly better than the 3LANPCC, showing that the lower number of semiconductor devices (i.e. 10 against 18) can offset the larger filter size requirement.

V. Conclusion

Nowadays, wide band-gap (WBG) devices are not yet widely adopted in variable-speed drive (VSD) applications, since their fast switching speeds can have harmful effects on the driven motor. To fully exploit their superior switching performance without increasing the machine stress, full differential-mode (DM) and common-mode (CM) sine-wave filtering at the converter output are considered. As a consequence, to reduce the impact of the sine-wave filter on the converter size and losses, higher switching frequencies and/or multi-level topologies need to be adopted.

This paper proposes a complete performance analysis of the most suited 2-L and 3-L SiC-based converters for VSD application. The stresses on the major active and passive converter components are investigated and compared, including the flux ripple in the DM and CM output inductors, the RMS current in the DC-link capacitors and the semiconductor losses. In particular, a novel analysis of the charge-related switching loss components is provided. The loss-optimal semiconductor chip area and the maximum efficiency of each converter solution are theoretically derived as functions of the operating switching frequency, considering a SiC-based 7.5 kW 800 V VSD. This analysis derives a theoretical upper limit to the performance of all topologies and allows to compare the flux-ripple stress applied to the output filter inductors of each solution for a given target efficiency, enabling a straightforward comparison between converters. Finally, a complete multi-objective optimization is carried out for each topology, aiming to maximize the efficiency and power density of the inverter including the output DM/CM sine-wave filter. The derived Pareto-optimal designs allow to better compare the achievable performance of the analyzed converter solutions. The T-type converter results the best performing candidate for the application at hand, both from the theoretical analysis and from the multi-objective optimization, achieving a volumetric power density of 37.8 $\mathrm{kW/dm^3}$ with an efficiency of 99.0 %, including the output sine-wave filter.

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