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ORIGINAL PAPER

Analysis and performance evaluation of a three-phase sparse neutral point clamped converter for industrial variable speed drives

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Abstract
This paper analyzes the operation and characterizes the performance of a three-phase three-level (3-L) Sparse Neutral Point Clamped converter (SNPCC) for industrial variable speed drives (VSDs). The operating principle of the SNPCC, which advantageously employs a lower number of power transistors than a conventional 3-L inverter, is described in detail, focusing on the AC-side differential-mode and common-mode voltage formation and on the DC-side mid-point current generation processes. The degrees of freedom in the SNPCC modulation scheme are defined and several switching sequences are investigated. Afterwards, the stresses on the active and passive components (e.g. semiconductor losses, machine phase current ripple, DC-link capacitor RMS current, etc.) are calculated by analytical and/or numerical means, enabling a straightforward performance comparison among the identified switching sequences. The most suited modulation strategy for VSD applications is then selected and a chip area sizing procedure, aimed at minimizing the total semiconductor chip size, is applied to a 800V 7.5kW three-phase system. The performance limits of the designed SNPCC are evaluated and finally compared to the ones of conventional 2-L and 3-L solutions, highlighting the promising cost/performance trade-off of the analyzed topology.

Keywords Sparse neutral point clamped converter · Industrial variable speed drives · Silicon IGBT · Semiconductor chip area

1 Introduction

Industrial variable speed drives (VSDs) and electric vehicle traction inverters [1] are highly cost sensitive and should show high reliability, which favors low-complexity, robust and proven inverter concepts based on silicon (Si) IGBTs. The conventional three-phase (3-Φ) two-level (2-L) inverter topology represents the de-facto industrial standard, due to its simplicity, low number of switches (i.e. 6 transistors and 6 diodes) and well understood operation [2]. However, when higher DC-link voltages are present, e.g. 800 V, the voltage rating of the devices must increase accordingly, leading to higher switching losses and larger overall semiconductor chip area. Three-level (3-L) inverters, such as the Neutral-Point Clamped (NPC) and T-Type topologies, represent excellent candidates for higher voltage drives, as they employ devices with reduced voltage ratings ensuring superior overall performance [3–5]. Moreover, taking advantage of the increased number of output voltage levels, they reduce the high-frequency harmonic current stress on the driven machine [6].

The Sparse Neutral Point Clamped converter (SNPCC) [7] illustrated in Fig. 1 has been introduced in [8] and represents a promising alternative to traditional 3-L inverters. The main advantage of the SNPCC resides in its lower number of active devices, i.e. 10 power transistors, compared to NPC and T-type 3-L converters, which both require at least 12 power transistors. On the other hand, the simpler converter structure translates in a lower number of switching states at high modulation indices [9], leading to slightly larger switching frequency output voltage harmonics. Due to its cascaded structure, composed of a 3-L switching matrix (SM) connected to a conventional 3-Φ 2-L inverter, the SNPCC lends itself to hybrid implementations. In particular, the 3-L SM and the 2-L inverter can conveniently adopt different semiconductor technologies (e.g. MOSFETs and IGBTs), since the former stage should maximize the switching per-

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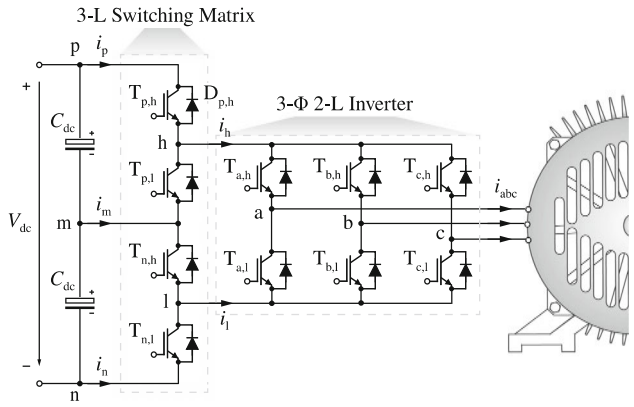

Fig. 1 Schematic of the Sparse Neutral Point Clamped converter (SNPCC). The cascaded structure composed of a three-level (3-L) switching matrix (SM) connected to a three-phase (3-Φ) two-level (2-L) inverter is highlighted. The diodes are named according to the paired transistors (see $D_{p,h}$)

formance, whereas the latter should minimize the conduction losses. Moreover, the complete converter can be integrated in a single power module, minimizing the commutation loop of the 2-L inverter devices, which includes two of the 3-L SM switches [10].

The operating principle and space vector modulation of the SNPCC have been analyzed in [8,9,11,12], while several control strategies for VSD applications are presented in [7,13–17]. Furthermore, the design of a hybrid GaN-Si SNPCC is reported in [10]. Nevertheless, according to the authors' best knowledge, a complete analysis of the converter component stresses and overall performance is not available in literature, especially considering the degrees of freedom associated with the converter modulation strategy. For instance, [9] identifies and compares several PWM pulse patterns with a different number of switching transitions, however only the effect on the low-frequency DC-link mid-point voltage oscillation is investigated, disregarding the induced switching frequency harmonic current stress on the driven machine and the switching losses in the semiconductor devices. Moreover, the analysis of [9] is limited to symmetric pulse patterns, hence excluding asymmetric ones, which can trade a higher sampling/control complexity for improved converter performance.

Accordingly, the main goals of this work are to provide a detailed analysis of the operation of the SNPCC, identify the most suitable symmetric and asymmetric modulation strategies for VSD application and derive the analytical and/or numerical expressions describing the stresses on the major active and passive components. These expressions quantitatively support the converter design, facilitating the sizing of DC-link capacitors, semiconductor devices and heatsink, and provide an indication of the spectrum of the converter 3-Φ output voltage, i.e. of the high-frequency harmonic stress on the driven machine. In particular, a complete performance comparison between modulation strategies over the full converter operating region is provided, taking into account the current ripple stress on the driven machine and the semiconductor switching losses. Moreover, a conclusive semiconductor chip area investigation aims to identify the cost/performance trade-off of the SNPCC, in comparison to traditional 2-L and 3-L solutions.

This paper is structured as follows. The operating principle of the SNPCC is described in Sect. 2. The converter switching states are identified and both the AC-side differential-mode (DM) and common-mode (CM) voltage formation and the DC-side mid-point current generation processes are explained. In Sect. 3, several suitable modulation strategies are defined, according to a set of rules constraining the switching sequence. In Sect. 4, the major component stresses, such as the machine phase current ripple, the DC-link capacitor RMS current and the semiconductor losses are investigated. In Sect. 5, a chip area minimization procedure is applied to three different 800V 7.5kW 3-Φ VSD systems, adopting a 2-L, a 3-L NPC and a 3-L SNPC converters, respectively. The performance limits of each topology are identified and compared, highlighting the promising cost/performance trade-off of the SNPCC. Finally, in Sect. 6, a brief summary of the main contributions of this work is provided. In the Appendix, further clarifications on the adopted analytical methods for the derivation of the machine phase current ripple and the converter switching losses are given.

2 Operating principle

The SNPCC is composed of a capacitively splitted DC input and a 3-L SM, i.e. a 3-L DC voltage source, feeding a 3-Φ 2-L inverter, as illustrated in Fig. 1. The role of the 3-L SM is to control the 2-L inverter rail-to-rail voltage v_{hl} in order to provide the desired 3-Φ output voltage in combination with the 2-L inverter. Due to the split DC-link, the 3-L SM semiconductor devices advantageously require only half the voltage rating of the 2-L inverter devices, resulting in lower on-state losses and higher switching speed.

2.1 Converter states

Because of its cascaded structure, the SNPCC offers a total of $2^2 \cdot 2^3 = 32$ conduction states [9]. While 18 of these combinations effectively apply a nonzero 3-Φ line-to-line output voltage (denominated *active* states), the remaining 14 combinations force a short-circuit of the 3-Φ output (denominated *zero* states). To avoid DC-link short circuits, only the combinations reported in Fig. 2a, b and c are allowed for the 3-L SM. Additionally, for reasons that will be clarified in Sect. 3,

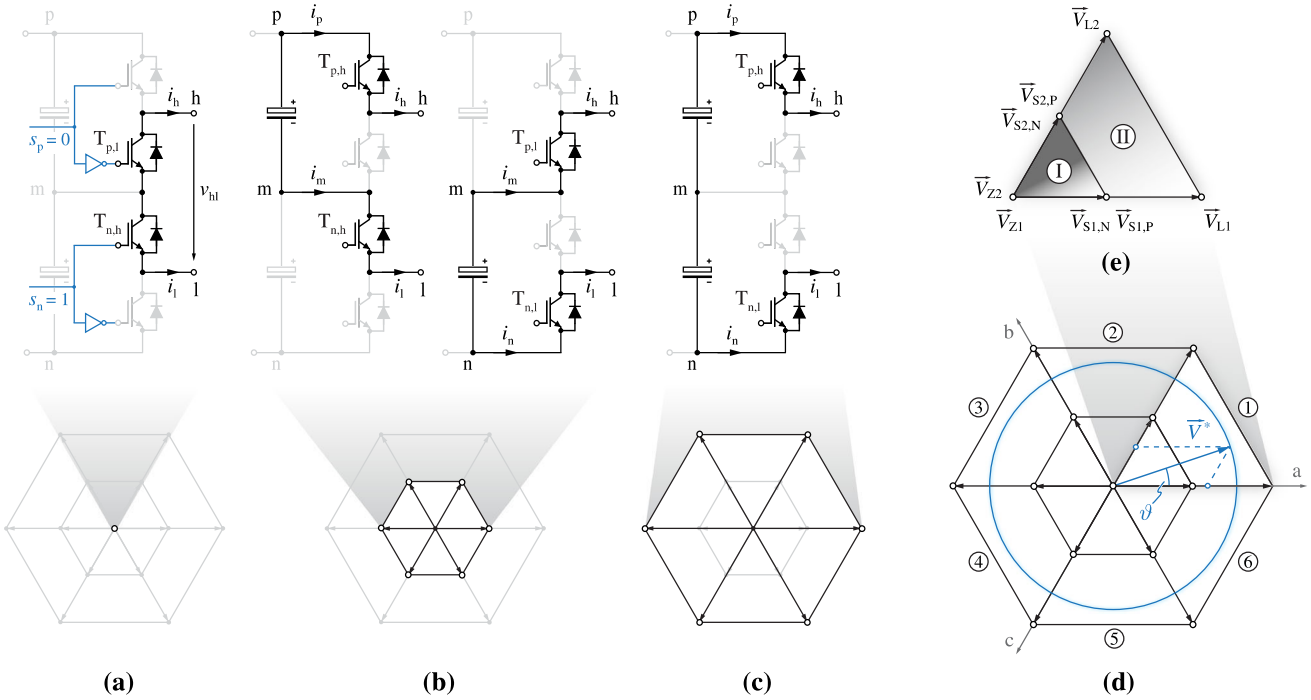

Fig. 2 Schematic of the 3-L switching matrix (SM) conduction states and respective SNPCC output voltage space vectors: **a** *zero* vector states, **b** *small* vector states and **c** *large* vector states. The complete SNPCC space vector hexagon is illustrated in (**d**), together with a reference voltage vector $\vec{V}^*$ and its decomposition. Sector ① and its subdivision in area Ⅰ and area Ⅱ are highlighted in (**e**) in combination with the associated *zero*, *small* and *large* vectors

the 2-L inverter *zero* states are not considered, thus the total count of *zero* states reduces to 6.

The converter states can be unequivocally identified by the 5 bridge-leg switching functions

$$s_x = \begin{cases} 0 & \text{if } T_{x,h} \text{ off}, \ T_{x,l} \text{ on} \\ 1 & \text{if } T_{x,h} \text{ on}, \ T_{x,l} \text{ off} \end{cases} \quad x = a, b, c, p, n. \tag{1}$$

By leveraging the relation between switching functions and bridge-leg voltages, the space vector representation of Fig. 2d can be finally obtained [9]. The main role of the 3-L SM is to synthesize the amplitude of the reference voltage vector $\vec{V}^*$, while the role of the 2-L inverter is to establish its direction. Three kinds of space vectors are identified and categorized according to their amplitude: *zero* vectors, *small* vectors with amplitude $V_{dc}/3$ and *large* vectors with amplitude $2V_{dc}/3$. The main difference between the SNPCC and standard 3-L inverters is the absence of *medium* vectors [18], which translates in a lower number of active states (18 against 24) and slightly higher switching frequency output voltage distortion.

For symmetry reasons, the converter operation can be completely analyzed inside a 60°-wide interval of a 3-Φ output period, i.e. a sector; sector ① is illustrated in Fig. 2e. Each sector can be divided in two main areas: area Ⅰ delimited by *zero* and *small* vectors, and area Ⅱ delimited by *small* and *large* vectors. The switching functions corresponding to the space vectors of sector ① are reported in Table 1. It can be observed that *small* vectors are redundant, since they can all be obtained with either of the two complementary states represented in Fig. 2b, both ensuring $v_{hl} = V_{dc}/2$.

Table 1 Bridge-leg switching functions, space vector amplitudes and converter rail currents corresponding to the space vectors of sector ①

Vector	s_a	s_b	s_c	s_p	s_n	$\lvert\vec{V}\rvert$	i_h	i_l	i_p	i_n	i_m
$\vec{V}_{Z1}$	1	0	0	0	1	0	$+i_a$	$-i_a$	0	0	0
$\vec{V}_{Z2}$	1	1	0	0	1	0	$-i_c$	$+i_c$	0	0	0
$\vec{V}_{S1,P}$	1	0	0	1	1	$\frac{V_{dc}}{3}$	$+i_a$	$-i_a$	$+i_a$	0	$-i_a$
$\vec{V}_{S1,N}$	1	0	0	0	0	$\frac{V_{dc}}{3}$	$+i_a$	$-i_a$	0	$-i_a$	$+i_a$
$\vec{V}_{S2,P}$	1	1	0	1	1	$\frac{V_{dc}}{3}$	$-i_c$	$+i_c$	$-i_c$	0	$+i_c$
$\vec{V}_{S2,N}$	1	1	0	0	0	$\frac{V_{dc}}{3}$	$-i_c$	$+i_c$	0	$+i_c$	$-i_c$
$\vec{V}_{L1}$	1	0	0	1	0	$\frac{2V_{dc}}{3}$	$+i_a$	$-i_a$	$+i_a$	$-i_a$	0
$\vec{V}_{L2}$	1	1	0	1	0	$\frac{2V_{dc}}{3}$	$-i_c$	$+i_c$	$-i_c$	$+i_c$	0

2.2 Space vectors dwell-time calculation [9]

Defining the converter modulation index $M = 2V^*/V_{dc}$, reporting the reference space vector angle ϑ in a $[0, 60°]$ window and leveraging simple geometrical relations, the dwell-time expressions

$$\text{Area } ① : \begin{cases} \delta_{S1}(\vartheta) = \sqrt{3}M \sin\left(\frac{\pi}{3} - \vartheta\right) \\ \delta_{S2}(\vartheta) = \sqrt{3}M \sin\left(\vartheta\right) \\ \delta_{Z}(\vartheta) = 1 - \delta_{S1}(\vartheta) - \delta_{S2}(\vartheta) \end{cases} \tag{2}$$

$$\text{Area } Ⅱ : \begin{cases} \delta_{S1}(\vartheta) = (2 - 3u)d_1 \\ \delta_{S2}(\vartheta) = (2 - 3u)d_2 \\ \delta_{L1}(\vartheta) = (3u - 1)d_1 \\ \delta_{L2}(\vartheta) = (3u - 1)d_2 \end{cases} \tag{3}$$

are obtained in sector ①, where

$$u = \frac{1}{\sqrt{3}} M \cos\left(\tfrac{\pi}{6} - \vartheta\right), \tag{4}$$

$$d_1 = \frac{\sin\left(\frac{\pi}{3} - \vartheta\right)}{\cos\left(\frac{\pi}{6} - \vartheta\right)}, \tag{5}$$

$$d_2 = \frac{\sin\left(\vartheta\right)}{\cos\left(\frac{\pi}{6} - \vartheta\right)}, \tag{6}$$

and the modulation index boundary between area Ⅰ and area Ⅱ is

$$M_{\text{lim}} = \frac{1}{\sqrt{3}\cos\left(\vartheta - \frac{\pi}{6}\right)}. \tag{7}$$

The dwell-time calculation in area Ⅱ assumes that no *small* or *large* vector can be avoided in a switching sequence. Even though area Ⅱ could be divided into sub-regions to reduce the minimum number of space vector transitions in a switching period [12], this would increase the degrees of freedom in the modulation strategy definition and considerably complicate the PWM and control processes, hence it is not considered herein.

2.3 DC-link mid-point current generation

In order to ensure a symmetric 3-L characteristic and a limitation of the blocking voltage stress on the 3-L SM switches to half of the total DC input voltage, the voltages V_{pm} and V_{mn} across the two series connected DC-link capacitors must be balanced [19], as described in the following.

The 2-L inverter rail current

$$i_{\text{h}} = s_{\text{a}} i_{\text{a}} + s_{\text{b}} i_{\text{b}} + s_{\text{c}} i_{\text{c}} = -i_{\text{l}} \tag{8}$$

allows to derive the 3-L SM rail currents

$$i_{\text{p}} = s_{\text{p}} i_{\text{h}} = s_{\text{p}}(s_{\text{a}} i_{\text{a}} + s_{\text{b}} i_{\text{b}} + s_{\text{c}} i_{\text{c}}), \tag{9}$$

$$i_{\text{n}} = (1 - s_{\text{n}})\, i_{\text{l}} = (s_{\text{n}} - 1)(s_{\text{a}} i_{\text{a}} + s_{\text{b}} i_{\text{b}} + s_{\text{c}} i_{\text{c}}), \tag{10}$$

$$i_{\text{m}} = -(i_{\text{p}} + i_{\text{n}}) = (1 - s_{\text{p}} - s_{\text{n}})(s_{\text{a}} i_{\text{a}} + s_{\text{b}} i_{\text{b}} + s_{\text{c}} i_{\text{c}}), \tag{11}$$

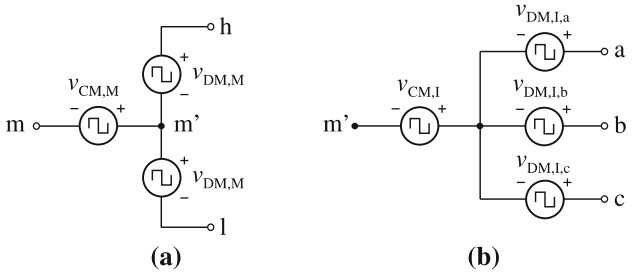

Fig. 3 Equivalent circuits of **a** the 3-L SM and **b** the 3-Φ 2-L inverter. The DM and CM components of the generated voltages are represented by ideal switched voltage sources

which are summarized in Table 1 (for sector ①). Only the *small* vectors affect the mid-point current i_{m}. In particular, the redundant vectors ($V_{\text{S1,P}}/V_{\text{S1,N}}$ and $V_{\text{S2,P}}/V_{\text{S2,N}}$) have an equal and opposite effect on i_{m}, allowing to balance the DC-link capacitor voltages V_{pm} and V_{mn}. If both redundant *small* vectors are used, the mid-point current local average (i.e. mean value over a switching period) in sector ① is

$$i_{\text{m,AVG}} = (1 - 2\alpha)(\delta_{\text{S1}}\, i_{\text{a}} - \delta_{\text{S2}}\, i_{\text{c}}), \tag{12}$$

where $\alpha \in [0,\ 1]$ is a control parameter which defines the dwell-time of the positive *small* vectors, i.e. $V_{\text{S1,P}}$ and $V_{\text{S2,P}}$, relative to the total *small* vector dwell-times δ_{S1} and δ_{S2}, respectively. In nominal operating conditions $\alpha = 0.5$ yields $i_{\text{m,AVG}} = 0$.

2.4 Output voltage formation

The converter 3-Φ output voltage derives from the superposition of both the 3-L SM and the 2-L inverter switching functions. Considering a balanced mid-point voltage $V_{\text{pm}} = V_{\text{mn}} = V_{\text{dc}}/2$,

$$v_{\text{xm}} = \frac{V_{\text{dc}}}{2}\left[s_{\text{p}} s_{\text{x}} + (1 - s_{\text{n}})(s_{\text{x}} - 1)\right] \quad \text{x} = \text{a, b, c} \tag{13}$$

is obtained. The DM component of v_{xm} defines the output voltage fundamental applied to the driven machine and the switching frequency voltage harmonics resulting in the phase current ripple (see Sect. 4), therefore it must be separated from the CM contribution. A straightforward approach considers the 3-L SM and 2-L inverter separately. The 3-L SM equivalent circuit is illustrated in Fig. 3a, where the virtual point m' is defined for the purpose of separating the DM and CM voltage sources into

$$v_{\text{DM,M}} = \frac{v_{\text{hm}} - v_{\text{lm}}}{2} = \frac{V_{\text{dc}}}{4}(s_{\text{p}} - s_{\text{n}} + 1) = \frac{v_{\text{hl}}}{2}, \tag{14}$$

$$v_{\text{CM,M}} = \frac{v_{\text{hm}} + v_{\text{lm}}}{2} = \frac{V_{\text{dc}}}{4}(s_{\text{p}} + s_{\text{n}} - 1). \tag{15}$$

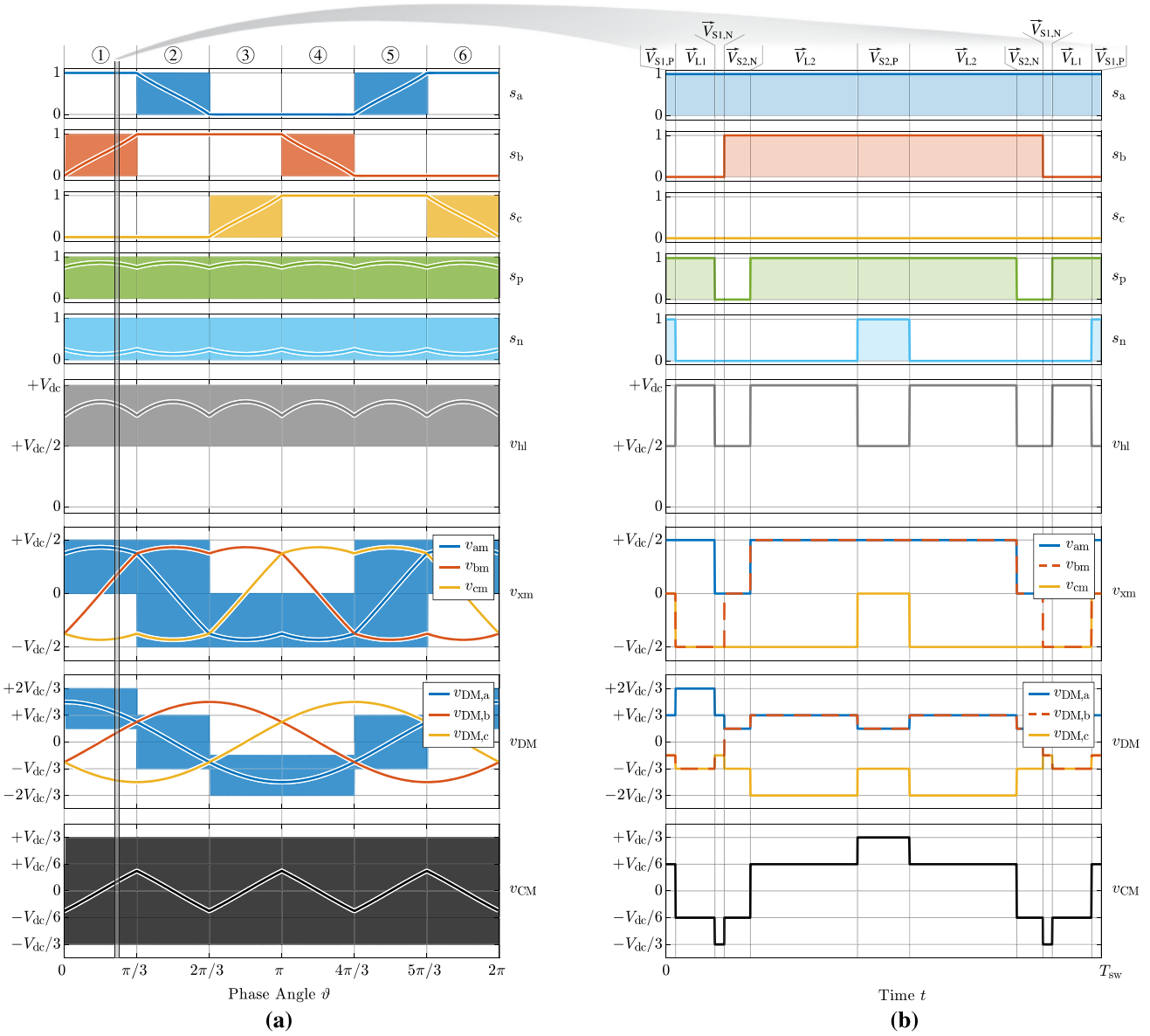

Fig. 4 Bridge-leg switching functions s_a, s_b, s_c, s_p, s_n and voltage waveforms v_{hl}, v_{am}, v_{bm}, v_{cm}, $v_{DM,a}$, $v_{DM,b}$, $v_{DM,c}$, v_{CM} in area Ⅱ ($M = 1$) **a** over a 3-Φ output period and **b** over a switching period in sector Ⅰ. Switching sequence U (see Sect. 3) is selected. In (**a**), the waveform local averages are superimposed to their instantaneous values for better understanding. The injected CM local average is the same as for standard space vector modulation

The 2-L inverter equivalent circuit is shown in Fig. 3b, where a second virtual point is arbitrarily defined coincident with m'. Both DM and CM contributions depend on $v_{hl} = 2\,v_{DM,M}$, in particular

$$v_{DM,I,x} = v_{xm'} - v_{CM,I} = v_{hl}\left(s_x - \frac{s_a + s_b + s_c}{3}\right), \tag{16}$$

$$v_{CM,I} = \frac{v_{am'} + v_{bm'} + v_{cm'}}{3} = \frac{v_{hl}}{6}\left[2(s_a + s_b + s_c) - 3\right]. \tag{17}$$

Finally, the total DM and CM voltages can be derived from (14)–(17), obtaining

$$v_{DM,x} = v_{DM,I,x} \quad x = a,\ b,\ c, \tag{18}$$

$$v_{CM} = v_{CM,M} + v_{CM,I}. \tag{19}$$

A summary of the DM and CM output voltages in sector Ⅰ is provided in Table 2. The DM voltage waveform $v_{DM,x}$ is composed of 5 levels in area Ⅰ and 6 levels in area Ⅱ, while the CM waveform v_{CM} shows 5 levels in area Ⅰ and 4 levels in area Ⅱ.

Table 2 2-L inverter rail-to-rail voltage and DM and CM output voltage components corresponding to the space vectors of sector Ⅰ

Vector	v_{hl}	$v_{CM,M}$	$v_{CM,I}$	$v_{DM,a}$	$v_{DM,b}$	$v_{DM,c}$	v_{CM}
$\vec{V}_{Z1}$	0	0	0	0	0	0	0
$\vec{V}_{Z2}$	0	0	0	0	0	0	0
$\vec{V}_{S1,P}$	$\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{4}$	$-\frac{V_{dc}}{12}$	$+\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{6}$	$+\frac{V_{dc}}{6}$
$\vec{V}_{S1,N}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{4}$	$-\frac{V_{dc}}{12}$	$+\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{3}$
$\vec{V}_{S2,P}$	$\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{4}$	$+\frac{V_{dc}}{12}$	$+\frac{V_{dc}}{6}$	$+\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{3}$	$+\frac{V_{dc}}{3}$
$\vec{V}_{S2,N}$	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{4}$	$+\frac{V_{dc}}{12}$	$+\frac{V_{dc}}{6}$	$+\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{6}$
$\vec{V}_{L1}$	V_{dc}	0	$-\frac{V_{dc}}{6}$	$+\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{6}$
$\vec{V}_{L2}$	V_{dc}	0	$+\frac{V_{dc}}{6}$	$+\frac{V_{dc}}{3}$	$+\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$+\frac{V_{dc}}{6}$

An example of the converter switching functions and voltage waveforms in area Ⅱ is provided in Fig. 4, where $M = 1$ is considered. These waveforms are obtained by ordering the space vectors according to a generic switching sequence (i.e. sequence U, see Sect. 3) and translating them into a pulse pattern in the time domain. It can be visualized that the 2-L inverter switching functions (s_a, s_b and s_c) are alternately clamped either to 0 or 1 for two-thirds of the fundamental period, as in the *1/3 Modulation* [20]. This behavior derives from avoiding the 2-L inverter *zero* states, which allows to switch only one inverter bridge-leg in each sector. To achieve 3-Φ sinusoidal (in local average) output voltages, the 3-L SM operates such that the local average of v_{hl} follows the 3-Φ rectified line-to-line output voltage fundamentals. In other words, in each sector, the 3-L SM sets the desired voltage between the two clamped phases, leaving to the third inverter bridge-leg the regulation of the two remaining 3-Φ line-to-line output voltages [20].

The local averages of v_{CM} and v_{xm} are the same as for the conventional space vector modulation, independently on the selected modulation strategy. This is because switching sequence U and all sequences described in Sect. 3 must include every available non-*zero* state and equally distribute the dwell-time between redundant *small* space vectors, thus yielding the same 3-Φ output voltage local average as a conventional 2-L inverter. Differently from 2-L and other 3-L inverters, the dwell-time allocation of the *zero* states does not influence the CM voltage, since both V_{Z1} and V_{Z2} result in $v_{CM} = 0\text{V}$.

The focus over a switching period in Fig. 4b provides insight into the selected switching sequence and allows to verify the DM and CM voltage levels listed in Table 2.

To conclude, the generated 3-Φ sinusoidal output and mid-point current waveforms with unity power factor ($\cos\varphi = 1$), i.e. ohmic load behavior, are illustrated in Fig. 5. The value of the machine phase inductance (acting as filtering element) is selected to achieve a 30% maximum peak-to-peak current ripple during a 3-Φ output period. While i_m continuously

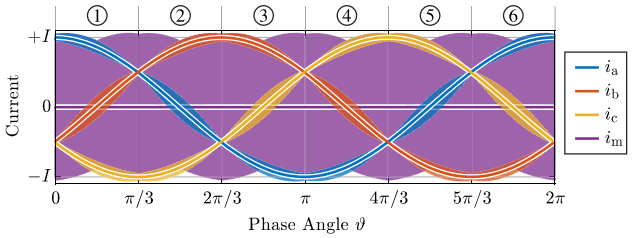

Fig. 5 3-Φ sinusoidal output currents i_a, i_b, i_c and mid-point current i_m waveforms with unity load power factor ($\cos\varphi = 1$) over a 3-Φ output period. Switching sequence U (see Sect. 3) is selected. Waveform local averages are superimposed to their instantaneous values for better understanding

jumps between two 3-Φ sinusoidal output currents and 0A, its local average is 0A during the complete 3-Φ output period. This behavior is maintained for all values of $\cos\varphi$, since complementary redundant *small* vectors are always opportunely applied, as explained in Sect. 3.

3 Modulation strategies

The reference space vector $\vec{V}^*$ (see Fig. 2d) can be synthesized in different ways, which give light to different modulation strategies. Both the switching sequence and the redundant *small* vector dwell-time allocation can be varied, yielding different results in terms of DM and CM voltage waveforms, semiconductor losses and mid-point current local average.

To limit the degrees of freedom in the modulation strategy definition, only switching sequences that

- have a single switching function change per vector transition,
- have less than 10 transitions per switching period,
- begin and end with the same *small* vector in order to avoid additional transitions between area Ⅰ and area Ⅱ,
- consider all redundant *small* vectors to have full control of the mid-point current local average ($\alpha = 0.5$ in steady state) and
- avoid the 2-L inverter *zero* states, since these would force additional switching transitions,

are considered throughout this work.

According to these hypotheses, the converter states can be displayed in grid arrangement as in Fig. 6, with two different grids for area Ⅰ and area Ⅱ, where V_{Z1} and V_{Z2} in the former are replaced by V_{L1} and V_{L2} in the latter. This representation, firstly proposed in [9], easily illustrates the admitted switching transitions for the 3-L SM (blue arrows) and the 2-L inverter (pink arrows). By means of simple geometrical considerations and aiming for the minimum number

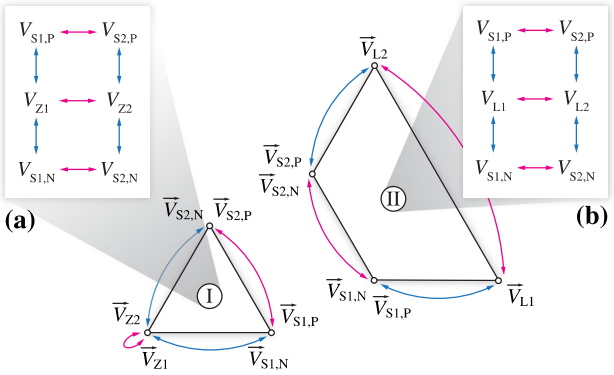

Fig. 6 Graphical representation of the admissible 2-L inverter (pink arrows) and 3-L SM (blue arrows) space vector transitions in **a** area Ⓘ and **b** area Ⓘ

of switching events, the switching sequences which comply with the mentioned hypotheses are identified and reported in Fig. 7 and in Table 3. The equivalent switching frequencies of the 3-L SM $f_{\mathrm{sw,M}}$ and the 2-L inverter $f_{\mathrm{sw,I}}$ in Table 3 (normalized with respect to the sampling/control frequency f_{s}) are found by averaging the switching frequencies of the respective transistors as

$$f_{\mathrm{sw,M}} = \frac{1}{4}\sum_{j=1}^{4} f_{\mathrm{sw,j}} \quad \text{and} \quad f_{\mathrm{sw,I}} = \frac{1}{6}\sum_{k=1}^{6} f_{\mathrm{sw,k}}, \qquad (20)$$

where $f_{\mathrm{sw,j}}$ and $f_{\mathrm{sw,k}}$ are the switching frequencies of the j-th transistor in the 3-L SM and the k-th transistor in the 2-L inverter, respectively.

A distinction must be made between switching sequences with symmetric and asymmetric pulse patterns. Symmetric sequences are mirrored with respect to their center, meaning that the first half of the sequence is repeated in inverse order in the second half of the switching period. This is not the case for asymmetric pulse patterns: as a consequence, there is no fixed point in time when the instantaneous current value equals its local average, thus regular sampling cannot be adopted. Nevertheless, this issue can be easily overcome by modern microcontrollers with built-in oversampling and averaging functions. Therefore, both symmetric (*C*, *U*, *S*, *G*) and asymmetric (*O*, *8*, *B*, *6*, *A*, *H*, *3*) sequences are considered in the present analysis.

Since the switching sequence starting vector (i.e. one of the four *small* vectors) can determine different switching losses and affect their distribution among the semiconductor devices, all four sequence variants are investigated. In general, it can be advantageous to adopt different variants of a sequence in consecutive sectors. In order to minimize the number of switching actions at the sector transitions, only sequences starting with $V_{\mathrm{S1,P}}/V_{\mathrm{S2,P}}$ or $V_{\mathrm{S1,N}}/V_{\mathrm{S2,N}}$ can be alternated, i.e. mirrored. This can reduce or eliminate uncontrollable current ripple spikes at the sector transitions, typically encountered when asymmetric pulse patterns are adopted. Although this measure does not eliminate the low-frequency harmonics in the output voltage waveform, inherent to asymmetric switching sequences, the resulting current distortion can be reduced with a properly tuned converter closed-loop control, comprising a disturbance feed-forward correction. In addition, it can be demonstrated that alternating complementary switching sequences between odd and even sectors allows to obtain symmetric switching loss characteristics with respect to the load power factor for all modulation strategies (see Fig. 14). For the mentioned reasons, the mir-

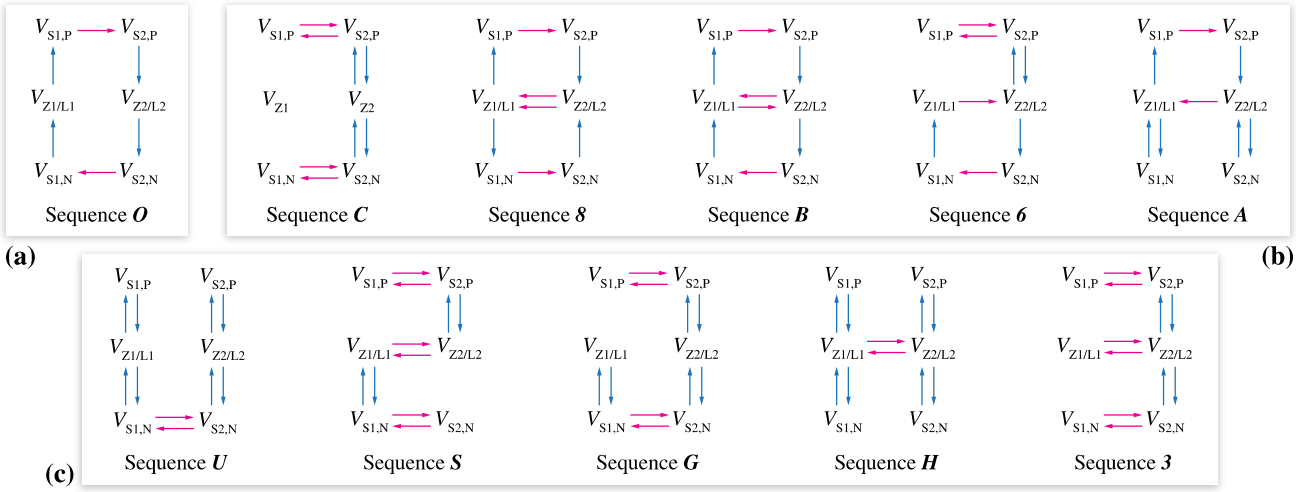

Fig. 7 Graphical representation of the most suitable symmetric and asymmetric switching sequences starting with $V_{\mathrm{S1,P}}$: **a** 6-transition sequence, **b** 8-transition sequences and **c** 10-transition sequences. The switching transitions involving the 3-L SM are represented by blue arrows, while pink arrows indicate the 2-L inverter transitions. Sequence *C* is only admitted in area Ⓘ, since no *large* vector can generally be avoided in area Ⓘ. Four times the displayed sequences are possible, since each sequence can be mirrored, i.e. can start with any *small* vector (grid corner)

Table 3 Overview of the considered symmetric (*C*, *U*, *S*, *G*) and asymmetric (*O*, *8*, *B*, *6*, *A*, *H*, *3*) switching sequences

Name	Transitions	Sequence	$f_{sw,M}/f_s$	$f_{sw,I}/f_s$
C	8	$V_{S1,P} \rightleftarrows V_{S2,P} \rightleftarrows V_{Z2} \rightleftarrows V_{S2,N} \rightleftarrows V_{S1,N}$	1	2/3
U	10	$V_{S1,P} \rightleftarrows V_{Z1/L1} \rightleftarrows V_{S1,N} \rightleftarrows V_{S2,N} \rightleftarrows V_{Z2/L2} \rightleftarrows V_{S2,P}$	2	1/3
S	10	$V_{S1,P} \rightleftarrows V_{S2,P} \rightleftarrows V_{Z2/L2} \rightleftarrows V_{Z1/L1} \rightleftarrows V_{S1,N} \rightleftarrows V_{S2,N}$	1	1
G	10	$V_{S1,P} \rightleftarrows V_{S2,P} \rightleftarrows V_{Z2/L2} \rightleftarrows V_{S2,N} \rightleftarrows V_{S1,N} \rightleftarrows V_{Z1/L1}$	3/2	2/3
O	6	$V_{S1,P} \rightarrow V_{S2,P} \rightarrow V_{Z2/L2} \rightarrow V_{S2,N} \rightarrow V_{S1,N} \rightarrow V_{Z1/L1} \rightarrow V_{S1,P}$	1	1/3
8	8	$V_{S1,P} \rightarrow V_{S2,P} \rightarrow V_{Z2/L2} \rightarrow V_{Z1/L1} \rightarrow V_{S1,N} \rightarrow V_{S2,N} \rightarrow V_{Z2/L2} \rightarrow V_{Z1/L1} \rightarrow V_{S1,P}$	1	2/3
B	8	$V_{S1,P} \rightarrow V_{S2,P} \rightarrow V_{Z2/L2} \rightarrow V_{Z1/L1} \rightarrow V_{Z2/L2} \rightarrow V_{S2,N} \rightarrow V_{S1,N} \rightarrow V_{Z1/L1} \rightarrow V_{S1,P}$	1	2/3
6	8	$V_{S1,P} \rightarrow V_{S2,P} \rightarrow V_{Z2/L2} \rightarrow V_{S2,N} \rightarrow V_{S1,N} \rightarrow V_{Z1/L1} \rightarrow V_{Z2/L2} \rightarrow V_{S2,P} \rightarrow V_{S1,P}$	1	2/3
A	8	$V_{S1,P} \rightarrow V_{S2,P} \rightarrow V_{Z2/L2} \rightarrow V_{S2,N} \rightarrow V_{Z2/L2} \rightarrow V_{Z1/L1} \rightarrow V_{S1,N} \rightarrow V_{Z1/L1} \rightarrow V_{S1,P}$	3/2	1/3
H	10	$V_{S1,P} \rightarrow V_{Z1/L1} \rightarrow V_{S1,N} \rightarrow V_{Z1/L1} \rightarrow V_{Z2/L2} \rightarrow V_{S2,N} \rightarrow V_{Z2/L2} \rightarrow V_{S2,P} \rightarrow V_{Z2/L2} \rightarrow V_{Z1/L1} \rightarrow V_{S1,P}$	2	1/3
3	10	$V_{S1,P} \rightarrow V_{S2,P} \rightarrow V_{Z2/L2} \rightarrow V_{Z1/L1} \rightarrow V_{Z2/L2} \rightarrow V_{S2,N} \rightarrow V_{S1,N} \rightarrow V_{S2,N} \rightarrow V_{Z2/L2} \rightarrow V_{S2,P} \rightarrow V_{S1,P}$	1	1

The equivalent switching frequencies of the 2-L inverter ($f_{sw,I}$) and the 3-L SM ($f_{sw,M}$) are reported in normalized form with respect to the sampling/control frequency f_s

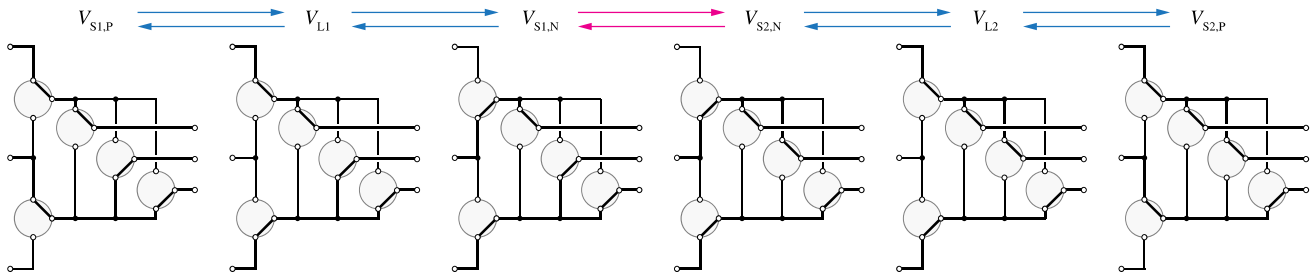

Fig. 8 Equivalent circuit representation of all converter conduction states in area Ⅱ of sector ①, ordered according to sequence *U*. Since sequence *U* is symmetric, the space vector pattern from $V_{S1,P}$ to $V_{S2,P}$ is repeated in the opposite direction during the second half of the switching period

roring of switching sequences is considered throughout this work, yielding results which are independent on the sequence starting vector and thus simplifying the analysis.

All the identified symmetric switching sequences (i.e. *C*, *U*, *S*, *G*) are also reported in [9], which additionally considers modulation strategies that do not ensure a zero mid-point current local average and that adopt the 2-L inverter *zero* states in area Ⅰ. For instance, sequence *U* is referred to as Maximum Neutral Point Balancing (MNPB) sequence in [9] and is tested experimentally on a SNPCC prototype in [10].

Finally, for completeness, an equivalent circuit representation of all converter conduction states in area Ⅱ of sector ①, ordered according to sequence *U*, is reported in Fig. 8.

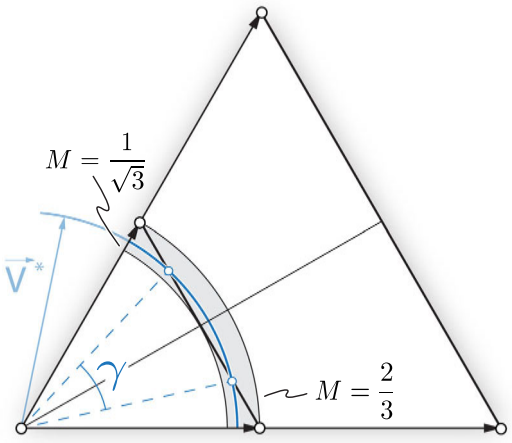

Fig. 9 Transition region between area Ⅰ and area Ⅱ in sector ①. The angle γ indicates the fraction of the reference space vector $\vec{V}^*$ trajectory situated inside area Ⅱ

4 Component stresses

The voltage and/or current stresses on the active and passive components have a direct impact on the converter design. Analytical and/or numerical expressions are derived in this section for all major component stresses, in relation with the adopted modulation strategy.

In the following calculations, the expressions of the 3-Φ sinusoidal output currents

$$\begin{aligned} i_a &= I\cos(\vartheta - \varphi), \\ i_b &= I\cos(\vartheta - \varphi - \tfrac{2}{3}\pi), \\ i_c &= I\cos(\vartheta - \varphi - \tfrac{4}{3}\pi), \end{aligned} \tag{21}$$

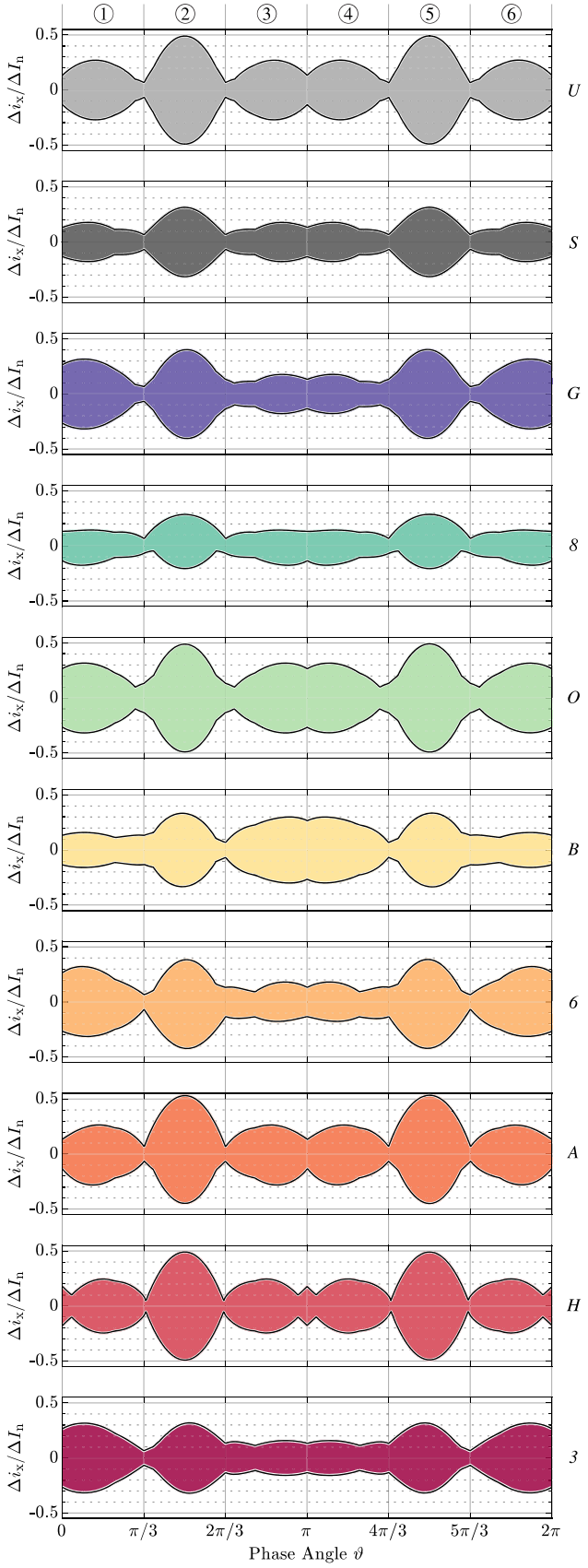

Fig. 10 Normalized output current ripple $\Delta i_x/\Delta I_n$ over a 3-Φ output period for $M = 0.85$. All switching sequences are displayed except for *C*, since $M > 1/\sqrt{3}$. The ripple waveforms related to sequences *8*, *6* and *A* are not half-wave symmetric and thus include even order switching harmonics

where φ is the load power factor angle, are considered.

Figure 9 highlights the transition region between area Ⓘ and area Ⓘⓘ in sector ①, i.e. the modulation index interval $1/\sqrt{3} \leq M \leq 2/3$ in which the reference space vector $\vec{V}^*$ crosses both areas. Since separate analytical expressions of the component stresses are derived for area Ⓘ and area Ⓘⓘ, a merging procedure must be performed in the transition region, in order to ensure the continuity of the results. Leveraging simple geometrical relations, the merged expression of the generic quantity X can be obtained as

$$X = X_{\text{Ⓘ}}\left(1 - \frac{\gamma}{\pi/3}\right) + X_{\text{Ⓘⓘ}}\frac{\gamma}{\pi/3} \quad 1/\sqrt{3} \leq M \leq 2/3, \tag{22}$$

where $X_{\text{Ⓘ}}$ and $X_{\text{Ⓘⓘ}}$ are the expressions in area Ⓘ and area Ⓘⓘ, respectively, and

$$\gamma = 2\cos^{-1}\left(\frac{1}{\sqrt{3}M}\right) \tag{23}$$

is the angle reported in Fig. 9.

4.1 Machine phase current ripple

The DM voltage-time area applied to the machine phases generates a switching frequency flux linkage ripple, which translates in a current ripple inversely proportional to the machine phase inductance L. This ripple is directly responsible for the high-frequency winding and iron losses in the machine itself [21], thus representing a first performance indicator of the adopted modulation strategy.

The current ripple of phase x is found by integrating the high-frequency component of the DM voltage $v_{\text{DM,x,hf}}$, i.e. subtracting the local average from v_{DM}, as

$$\Delta i_x(t) = \frac{1}{L}\int_0^t v_{\text{DM,x,hf}}\,\mathrm{d}t \quad \text{x} = \text{a, b, c.} \tag{24}$$

This modeling approach has been adopted and experimentally validated in [22], demonstrating a high level of accuracy.

A highlight of the output current ripple waveforms is provided in Fig. 10, assuming $M = 0.85$. To generalize the results, the normalization factor

$$\Delta I_n = \frac{V_{dc}}{8\, f_{sw}\, L} \tag{25}$$

is introduced [23] and the current ripple waveforms are expressed in normalized form. It is worth observing that some asymmetric switching sequences (e.g. *8*, *6*, *A*) yield a current ripple envelope that lacks half-wave symmetry, thus featuring an output current spectrum with even order switching harmonics, neverthless, these harmonics do not affect the low-frequency sinusoidal output current shape.

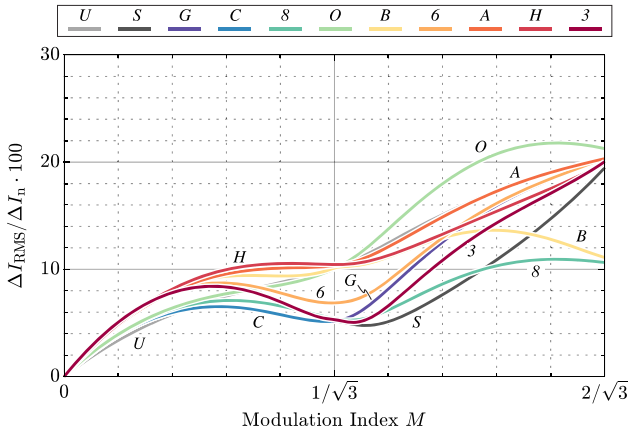

Fig. 11 Normalized total RMS machine phase current ripple $\Delta I_{\mathrm{RMS}}/\Delta I_{\mathrm{n}}$ as a function of the modulation index M and the switching sequence

To take into account the complete 3-Φ output period, the total RMS current ripple is considered as performance index. Its value can be derived by averaging the RMS current ripple contributions of all three phases over one sector as

$$\Delta I_{\mathrm{RMS}}^2 = \frac{6}{T}\int_0^{T/6} \frac{\Delta i_{\mathrm{a}}^2 + \Delta i_{\mathrm{b}}^2 + \Delta i_{\mathrm{c}}^2}{3}\,\mathrm{d}t. \tag{26}$$

It is easily proven that ΔI_{RMS} is independent on the starting vector of the switching sequence. Separate ΔI_{RMS} analytical expressions can be derived for area Ⓘ and area ⒾⒾ, as described in Appendix 1. Therefore, to ensure the continuity of the results over the complete modulation index M range, the merging procedure previously described is applied.

The normalized total RMS current ripples generated by the different modulation strategies are reported in Fig. 11. A best performing sequence cannot be identified over the full operating range, since ΔI_{RMS} depends on M. Nevertheless, an overall satisfactory trend is offered by sequence *8*, which yields the lowest ΔI_{RMS} value for high modulation indices.

4.2 DC-Link capacitor RMS current

Disregarding the switching frequency current ripple, the RMS current flowing into each DC-link capacitor in balanced conditions is not affected by the modulation strategy, since it only depends on the space vector dwell-times, as discussed in the following. Leveraging the sector periodicity, the expressions for the DC-link upper-rail current i_{p}, i.e.

$$I_{\mathrm{p,AVG}} = \frac{3}{\pi}\int_0^{\pi/3} i_{\mathrm{p,AVG}}\,\mathrm{d}\vartheta = \frac{3}{4} M I \cos\varphi, \tag{27}$$

$$I_{\mathrm{p,RMS}}^2 = \frac{3}{\pi}\int_0^{\pi/3} i_{\mathrm{p,RMS}}^2\,\mathrm{d}\vartheta = \frac{\sqrt{3}}{4\pi} M I^2 (4\cos^2\varphi + 1), \tag{28}$$

are obtained, where, focusing on sector Ⓘ,

$$i_{\mathrm{p,AVG}} = (\delta_{\mathrm{S1,P}} + \delta_{\mathrm{L1}})\, i_{\mathrm{a}} - (\delta_{\mathrm{S2,P}} + \delta_{\mathrm{L2}})\, i_{\mathrm{c}}, \tag{29}$$

$$i_{\mathrm{p,RMS}}^2 = (\delta_{\mathrm{S1,P}} + \delta_{\mathrm{L1}})\, i_{\mathrm{a}}^2 + (\delta_{\mathrm{S2,P}} + \delta_{\mathrm{L2}})\, i_{\mathrm{c}}^2. \tag{30}$$

Therefore, the same DC-link capacitor RMS current as for conventional 2-L and 3-L inverters results [24,25], i.e.

$$\begin{aligned} I_{C_{\mathrm{dc}},\mathrm{RMS}}^2 &= I_{\mathrm{p,RMS}}^2 - I_{\mathrm{p,AVG}}^2 \\ &= M I^2 \left[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}}{\pi} - \frac{9M}{16}\right)\right]. \end{aligned} \tag{31}$$

Even though $I_{C_{\mathrm{dc}},\mathrm{RMS}}$ is independent on the modulation strategy, the voltage ripple on C_{dc} generally depends on the switching sequence itself. Nevertheless, since all the strategies considered in this work force a zero mid-point current local average, no low-frequency mid-point voltage ripple is present, making a comparison between switching sequences unnecessary in these regards.

4.3 Semiconductor devices

4.3.1 Conduction losses

Silicon IGBTs and diodes are considered throughout this work. Their conduction characteristics can be approximated with a constant forward voltage drop term V_{th} and a differential resistance term R, as illustrated in Fig. 12a. Therefore, their conduction losses can be expressed by

$$P_{\mathrm{cond}} = V_{\mathrm{th}}\, I_{\mathrm{AVG}} + R\, I_{\mathrm{RMS}}^2, \tag{32}$$

where I_{AVG} and I_{RMS} are the average and RMS currents flowing through each device, respectively.

Disregarding the switching frequency current ripple, both I_{AVG} and I_{RMS} can be analytically derived for every device. This approach has been largely adopted in literature and its accuracy has been experimentally proven, e.g. in [26]. Different analytical expressions are found, depending on whether the reference voltage vector lies in area Ⓘ or area ⒾⒾ, therefore the merging of the results is applied in the transition region. Due to the complex nature of the derived expressions, these are not reported herein, nevertheless the IGBT current stresses are illustrated in Fig. 13

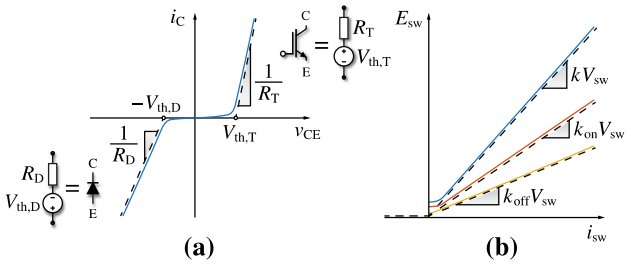

Fig. 12 Details on the considered IGBT/diode pair model. **a** Forward and reverse conduction characteristics and **b** switching energy characteristic divided in turn-on (including diode reverse-recovery), turn-off and total losses

in normalized form, as a function of M and φ. The current stresses in the paired diodes are identical, but shifted by $\varphi = \pi$.

It can be demonstrated that none of the expressions of I_{AVG} and I_{RMS} depends on the utilized switching sequence. Only if the 2-L inverter *zero* states were to be adopted, the conduction losses of the 3-L SM would depend on the modulation strategy, since during the 2-L inverter *zero* states none of the 3-L SM devices would be conducting.

4.3.2 Switching losses

The converter switching losses and their distribution between the 2-L inverter and the 3-L SM strongly depend on the selected switching sequence, since transitioning from a converter state to another can result in a more or less lossy commutation depending on the switched voltage and switched current values, as shown in Appendix 2. It can be easily demonstrated that the total converter switching losses have sector periodicity. Additionally, sequences *G*, *C*, *8*, *6*, *A* and *3* show different switching performance depending on the sequence starting vector. Nevertheless, by varying the starting vector between odd and even sectors as described in Sect. 3, this difference averages out over one 3-Φ output period, resulting in a symmetrical switching loss characteristic with respect to the load power factor angle φ.

To gain a quantitative insight into the switching performance of the SNPCC, the simplified energy loss model illustrated in Fig. 12b, based on a linear dependence with respect to both switched voltage V_{sw} and current i_{sw}, is adopted. Two different coefficients are identified for the turn-on (k_{on}) and the turn-off (k_{off}) transitions, leading to different loss components, i.e.

$$E_{\mathrm{on}} = k_{\mathrm{on}}\, V_{\mathrm{sw}}\, i_{\mathrm{sw}} \quad \text{and} \quad E_{\mathrm{off}} = k_{\mathrm{off}}\, V_{\mathrm{sw}}\, i_{\mathrm{sw}}, \tag{33}$$

where k_{on} includes the diode reverse-recovery loss contribution. If both transitions occur with the same V_{sw} and i_{sw} values, the total switching losses can be summarized as

$$E_{\mathrm{sw}} = k\, V_{\mathrm{sw}}\, i_{\mathrm{sw}}, \tag{34}$$

where $k = k_{\mathrm{on}} + k_{\mathrm{off}}$ and its value is assumed to only depend on the semiconductor voltage rating, as explained in Sect. 5.

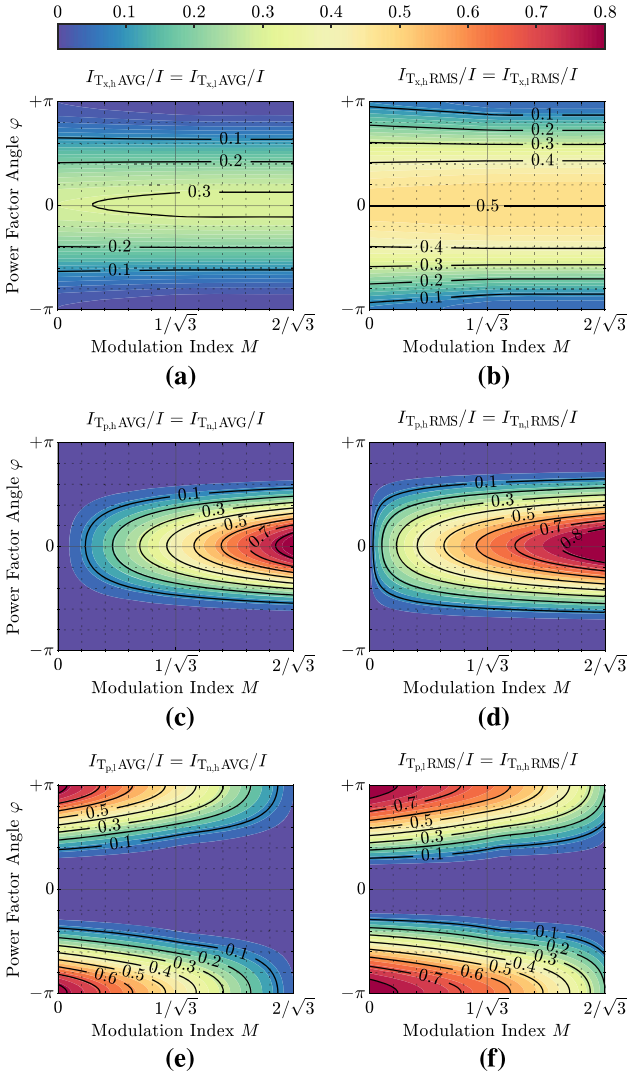

Fig. 13 Normalized I_{AVG} and I_{RMS} flowing through **a**, b the 2-L inverter transistors and **c**, **d**, **e**, **f**, the 3-L SM transistors, as a function of the modulation index M and the power factor angle φ (normalization with respect to I). The same current values apply to the respective diodes, however the results are shifted by $\varphi = \pi$. The current stresses in the 2-L inverter devices are mostly independent on M, as for conventional 2-L inverters [24], while the current stresses in the 3-L SM devices strongly depend on both M and φ. The maximum stress in these devices is always found for $\varphi = 0$ or $\varphi = \pi$, since the average and RMS values of the current flowing into the 3-L SM (i.e. i_{h}) are highest when the power transfer is maximized (i.e. $\cos\varphi = \pm 1$). Moreover, the value of M varies the conduction time intervals of the 3-L SM internal devices ($\mathrm{T_{p,h}}$, $\mathrm{T_{n,l}}$) and external devices ($\mathrm{T_{p,l}}$, $\mathrm{T_{n,h}}$), maximizing their current stresses for $M = 0$ and $M = 2/\sqrt{3}$, respectively

Table 4 SNPCC specifications and nominal operating conditions

Parameter	Description	Value
V_{dc}	DC-link voltage	800 V
M	Modulation index	0.85
V	Peak output phase voltage	340 V
I	Peak output phase current	14.7 A
$\cos\varphi$	Power factor	1
P	Output power	7.5 kW
f	Output frequency	0 . . . 300 Hz

The main goal of the considered simplified loss model is to enable a straightforward comparison among switching sequences. Nevertheless, the adopted linear switching loss approximation is met for most commercial IGBT/diode pairs, as attested by the switching loss data provided by the main manufacturers [27,28].

Disregarding the switching frequency current ripple and analyzing all vector transitions in each switching sequence, it is possible to express the 3-L SM and 2-L inverter switching losses analytically in closed form, as described in Appendix 2. The results of this analysis are independent on the semiconductor chip area (see Sect. 5) and are shown in normalized form in Fig. 14 as a function of φ, considering the values of k_{on}, k_{off} and k reported in Table 5. The switching loss subdivision between the 3-L SM and the 2-L inverter is derived for sequence *8* for demonstration purposes and is graphically illustrated in Fig. 21. Since separate analytical expressions are found for area Ⅰ and area Ⅱ, the switching losses in the transition region can be calculated with the previously reported merging procedure. Even though no single best solution is identified, sequence *O* results the best candidate over the full operating range for high M values, i.e. in area Ⅱ, since it avoids the most lossy switching transitions between *large* vectors.

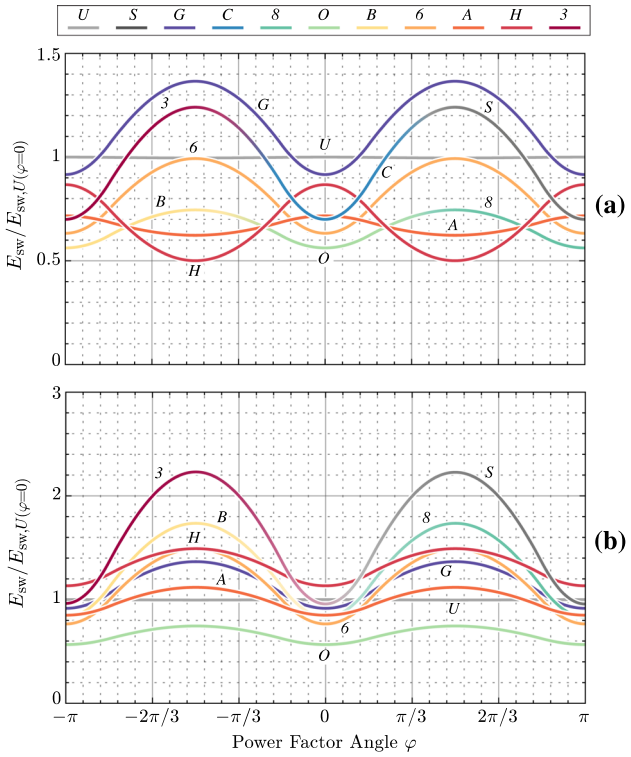

Fig. 14 Switching losses in **a** area Ⅰ and **b** area Ⅱ, normalized with respect to the switching losses of sequence U at $\varphi = 0$ in each area. The analytical derivation of these expressions is provided in Appendix 2. Some modulation strategies, i.e. *S-C-3*, *B-O-8* in area Ⅰ and *S-3*, *B-8* in area Ⅱ, yield identical switching losses and are thus superimposed. The highest switching loss values are encountered in area Ⅱ, since the $V_{Z1} \leftrightarrow V_{Z2}$ lossless transitions (i.e. $V_{sw} = 0$) are replaced by $V_{L1} \leftrightarrow V_{L2}$ (i.e. $V_{sw} = V_{dc}$). Therefore, all sequences which include these transitions are strongly favored or penalized depending whether the SNPCC is operating in area Ⅰ or area Ⅱ, respectively. The switching loss maxima in correspondence of $\varphi = \pm\pi/2$ are directly related to the 2-L inverter devices, since the two 30° switching windows of each bridge-leg (see Fig. 4a) become aligned with the respective phase current positive and negative peaks, thus maximizing the averaged switched current

5 Converter sizing and performance evaluation

The sizing and the performance evaluation of a 7.5kW 3-Φ SNPCC for VSD applications are described in the following, leveraging the analysis presented in the previous sections. The converter specifications and nominal operating conditions are summarized in Table 4.

5.1 Optimal modulation strategy

As discussed in Sect. 4, the performance of the switching sequences is summarized by ΔI_{RMS} in Fig. 11 and E_{sw} in Fig. 14. To compare them, an appropriate switching frequency f_{sw} is selected for each sequence to equalize the switching losses in nominal operating condition. Since ΔI_{RMS} is inversely proportional to f_{sw}, this process allows to obtain a single normalized performance index, providing a clear relative comparison between modulation strategies.

This comparison is performed assuming nominal operating conditions (i.e. $M = 0.85$, $\cos\varphi = 1$) and the results are illustrated in Fig. 15a, where lower index values translate into better performance. Figure 15b and c report the adjusted switching frequency values of both converter stages and the switching loss distribution between the 3-L SM and the 2-L inverter, respectively. It is shown that the relation between the switching frequency of a converter stage and its switching losses is not straightforward, as the results are also affected by the switched current and voltage values (see Appendix 2).

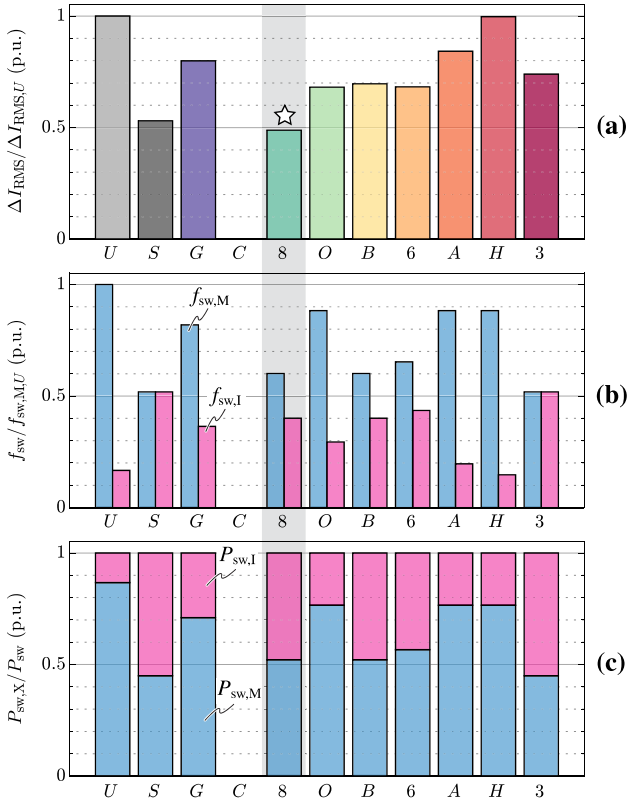

Fig. 15 **a** Total RMS current ripple normalized with respect to sequence U $\Delta I_{\mathrm{RMS}}/\Delta I_{\mathrm{RMS},U}$ for nominal operation ($M = 0.85$, $\cos\varphi = 1$), after adjusting the switching frequency f_{sw} of all modulation strategies in order to equalize the total switching losses. The adjusted switching frequency values (normalized with respect to the SM frequency in sequence U) and the switching loss subdivision between the two converter stages are reported in (**b**) and (**c**), respectively. All results are expressed in per unit (p.u.). Sequence C is not present since $M > 1/\sqrt{3}$, while sequence 8 is the best performing ($\star$)

Overall, the best performing switching sequence in the considered working point is the asymmetric sequence 8. Even though sequence S shows similar performance, i.e. achieving the best results among symmetric sequences, it features wider variations of $\Delta I_{\mathrm{RMS}}(M)$ (see Fig. 11) and $E_{\mathrm{sw}}(\varphi)$ (see Fig. 14) with respect to sequence 8, thus leading to a larger converter oversizing if a wide range of operating points needs to be covered.

5.2 Minimum semiconductor chip area

Depending on the operating point of the SNPCC, the current flowing through the semiconductor devices can be unevenly distributed, as shown in Fig. 13. This, together with the different conduction and switching characteristics of IGBTs and diodes, can lead to the unbalanced loading of certain devices. Therefore, the required chip area for each semiconductor device is investigated herein.

The basic concept behind the described chip area minimization procedure is to adapt the chip size of each semiconductor device based on its power losses, aiming to comply with a predefined maximum operating junction temperature. For instance, devices which are subject to higher current stresses require a larger chip size to reduce both the differential electrical resistance (lower conduction losses) and the thermal resistance (improved heat dissipation). Therefore, to quantitatively determine the minimum required chip area, accurate semiconductor loss and thermal models need to be defined.

The conduction characteristics of IGBTs and diodes are approximated as in Fig. 12. Considering R inversely proportional to the chip area A leads to the instantaneous conduction losses

$$p_{\mathrm{cond}} = V_{\mathrm{th}}\, i + \frac{R^*}{A}\, i^2, \tag{35}$$

where i is the conducted current and R^* is the IGBT/diode specific differential resistance (actual resistance multiplied with the chip area, which results in an area-independent characteristic figure, as known from unipolar power transistors [29]). By substituting in (35) the average and RMS current values derived in Sect. 4, the average conduction losses P_{cond} are obtained.

The selected switching loss model is described by (33) and (34), which assumes that all losses occur inside the IGBT. The proportionality terms k_{on}, k_{off} and k are considered to be independent on A, as assumed in [6] and [30]. The average switching losses of a single device can be calculated numerically by identifying all hard turn-on and turn-off transitions within a 3-Φ output period $T = 1/f$, together with the switched voltage V_{sw} and current i_{sw} values, as

$$P_{\mathrm{sw}} = \frac{1}{T}\left(\sum_{j=1}^{N_{\mathrm{on}}} k_{\mathrm{on}}\, V_{\mathrm{sw,j}}\, i_{\mathrm{sw,j}} + \sum_{k=1}^{N_{\mathrm{off}}} k_{\mathrm{off}}\, V_{\mathrm{sw,k}}\, i_{\mathrm{sw,k}}\right), \tag{36}$$

where N_{on} and N_{off} are respectively the number of hard turn-on and turn-off commutations of the considered device within T. It is important to separately calculate the switching losses for each device, since asymmetrical switching sequences can lead to an uneven loss distribution between devices of the same bridge-leg.

The junction-to-heatsink thermal resistance R_{th} model accounting for heat-spreading proposed in [31], i.e.

$$R_{\mathrm{th,}\,[\mathrm{K/W}]} = 23.94\, A_{[\mathrm{mm}^2]}^{-0.88}, \tag{37}$$

is finally considered. Each semiconductor junction temperature can thus be calculated as

$$T_{\mathrm{j}} = T_{\mathrm{hs}} + R_{\mathrm{th}}\, P_{\mathrm{tot}}, \tag{38}$$

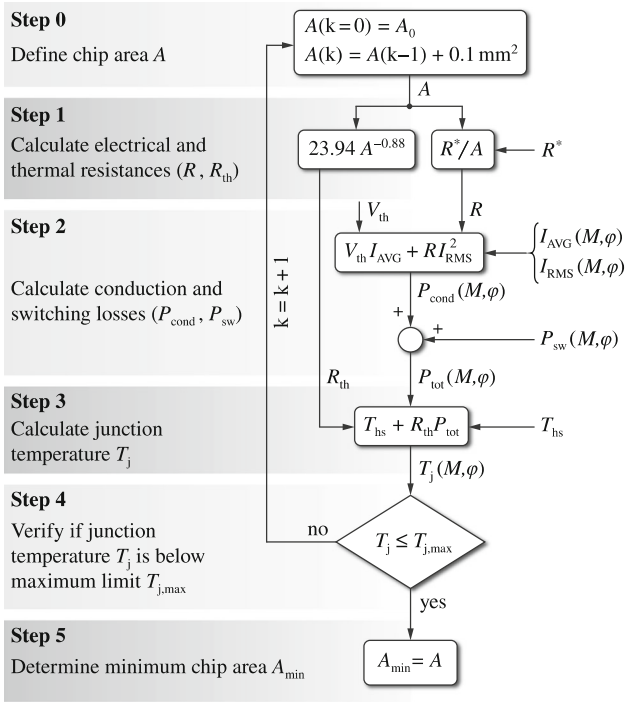

Fig. 16 Flow-chart of the adopted chip area minimization algorithm

where $T_{hs} = 80°C$ is the heatsink temperature and $P_{tot} = P_{cond} + P_{sw}$ is the average power loss in each device.

Leveraging these chip area dependent loss and thermal models, the algorithm used for determining the minimum required chip size illustrated in Fig. 16 is adopted. The semiconductor loss parameters V_{th}, R^* and k provided in Table 5 are obtained by statistical fitting of the conduction and switching characteristics of the latest generation 600/1200 V Trench and Field-Stop IGBTs and fast-recovery emitter-controlled diodes from Infineon [28]. Since these parameters are temperature dependent, the maximum admitted semiconductor junction temperature $T_{j,max} = 125°C$ is assumed as operating temperature from the beginning of the procedure, so that no additional iterative loop is required. A starting chip area value $A_0 = 4mm^2$ is considered due to practical manufacturing and wire-bonding limitations. Then, the chip size dependent electrical and thermal resistances are calculated, and the average conduction and switching losses in the design operating point are derived, leveraging the current stress and switching energy expressions obtained in Sect. 4. Finally, the chip junction temperature is calculated and compared to the maximum admitted value $T_{j,max}$. If the maximum temperature limit is fulfilled, the chip area value is saved and the algorithm is ended, otherwise the chip size is increased and the procedure is repeated.

The chip area minimization algorithm is run for the nominal operating point and different values of f_{sw}, selecting the minimum required chip size for each device to operate the converter at $M = 0.85$ and $\cos\varphi = 1$. By summing all IGBT and diode chip sizes, the total converter chip area is obtained.

Table 5 Loss parameters of the selected IGBT and diode technologies, considering $T_j = 125°C$

Device	V_{th}	R^*	k_{on}	k_{off}	k
M					
600 V IGBT	0.80 V	0.48 mm^2	83 ns	92 ns	175 ns
600 V Diode	0.75 V	0.32 mm^2	–	–	–
L					
1200 V IGBT	0.90 V	1.14 mm^2	188 ns	158ns	346ns
1200 V Diode	0.80 V	0.54 mm^2	–	–	–

M and I refer to the 3-L SM and 2-L inverter devices, respectively

5.3 Performance comparison

Following the described chip area minimization procedure, the SNPCC is compared to the most adopted converter topologies in industrial VSDs, namely the conventional 2-L converter and the 3-L NPC converter.

Figure 17a and b shows the trends of the total RMS current ripple ΔI_{RMS} and the total semiconductor chip area A_S as functions of f_{sw}, assuming conventional space vector modulation for the 2-L and the 3-L NPC converters, while considering switching sequence *8* for the SNPCC. The results obtained for the traditional 2-L and 3-L converter topologies are in good agreement with [6]. As a further confirmation of the adopted methodology, the minimum chip sizes obtained for all IGBTs result in device RMS current densities in the range of 80–120 A/mm^2, depending on the semiconductor breakdown voltage (i.e., 600 V, 1200 V) and the switching frequency (i.e., which determines switching losses). This is in close agreement with the typical value of around 100 A/mm^2 at nominal current for IGBTs of these voltage classes [32]. It is observed that the 3-L NPC yields both the minimum ΔI_{RMS} and the lowest chip area increase with f_{sw}. Nevertheless, the SNPCC requires a lower A_S at low frequencies, since it features less semiconductor devices. If a conventional 16 kHz operating switching frequency is assumed for the 2-L converter, the switching frequencies of the 3-L NPC and 3-L SNPC converters can be adjusted to ensure the same ΔI_{RMS} stress on the driven machine. This calculation process is graphically illustrated in Fig. 17 and the results are reported in Table 6.

The 2-L converter shows the worst overall performance, as already expected from previous analyses [3,5,6]. The 3-L SNPCC instead requires the lowest total semiconductor chip area and offers an efficiency comparable to the one of the 3-L NPC converter. Moreover, due to its lower number of transistors, it requires 2 less gate driver circuits, as well as 6 less diodes, further reducing the total part count

Table 6 Chip area and performance comparison between the 2-L, 3-L NPC and 3-L SNPC (switching sequence *8* is selected) converters, considering $P = 7.5\text{kW}$, $V_{\text{dc}} = 800\text{V}$, $M = 0.85$ and $\cos\varphi = 1$

Parameter	Description	2-L	3-L NPC	3-L SNPC Converter		
		Converter	Converter	2-L Inverter	3-L Matrix	Total
f_{sw}	Switching frequency	16 mm^2	7 kHz	6 kHz	9 kHz	9 kHz
A_{T}	Total transistor chip area	124 mm^2	66.0 mm^2	54.9 mm^2	36.4 mm^2	91.3 mm^2
A_{D}	Total diode chip area	24.0 mm^2	72.0 mm^2	24.0 mm^2	16.8 mm^2	40.8 mm^2
A_{S}	Total semiconductor chip area	148 mm^2	138 mm^2	78.9 mm^2	53.2 mm^2	132 mm^2
P_{cond}	Conduction losses	46.7 W	100 W	65.6 W	37.3 W	103 W
P_{sw}	Switching losses	124 W	13.7 W	14.0 W	15.3 W	29.3 W
P_{semi}	Semiconductor losses	171 W	114 W	79.6 W	52.6 W	132 W
η_{semi}	Semiconductor efficiency	97.8%	98.5%	99.0%	99.3%	98.3%

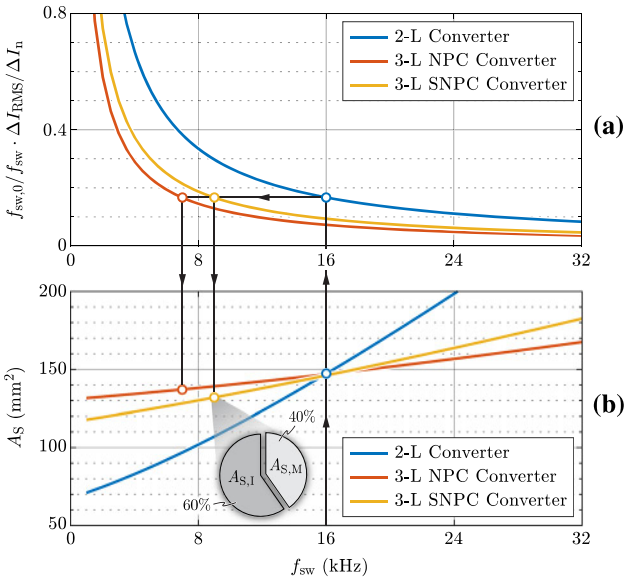

Fig. 17 **a** Normalized RMS phase current ripple $\Delta I_{\text{RMS}}/\Delta I_{\text{n}}$ multiplied by $f_{\text{sw,0}}/f_{\text{sw}}$ (i.e. $f_{\text{sw,0}} = 16\,\text{kHz}$ is a reference switching frequency purely defined for normalization purposes) and **b** total semiconductor chip area A_{S} as functions of the converter switching frequency f_{sw} for the 2-L, 3-L NPC and 3-L SNPC converters, considering $P = 7.5\,\text{kW}$, $V_{\text{dc}} = 800\,\text{V}$, $M = 0.85$ and $\cos\varphi = 1$. Conventional space vector modulation is assumed for the 2-L and 3-L NPC converters, while switching sequence *8* is considered for the SNPCC. A cross-over between the three A_{S} curves is observed in (**b**), around $f_{\text{sw}} = 16\,\text{kHz}$, clearly defining the topology with the lowest chip area requirement over the complete frequency range. The design point for each converter is obtained adjusting f_{sw} to yield the same ΔI_{RMS}, assuming the 2-L converter operated at 16 kHz as reference design. This procedure is illustrated graphically, resulting in $f_{\text{sw}} = 7\,\text{kHz}$ for the 3-L NPC converter and in $f_{\text{sw}} = 9\,\text{kHz}$ for the 3-L SNPCC (i.e. $f_{\text{sw}} = f_{\text{s}}$, cf. Table 3). A complete comparison of the performance results is reported in Table 6. The SNPCC total semiconductor area is divided between the 2-L inverter ($A_{\text{S,I}}$) and the 3-L SM ($A_{\text{S,M}}$), as highlighted in the pie chart

and overall complexity. Therefore, the SNPCC represents a promising alternative to traditional industrial VSD solutions, particularly in those applications which require relatively low switching frequency. The results of this analysis substantiate and supplement the findings reported in [9,10].

To further enhance the performance comparison among the 3-L SNPC switching sequences, the chip area minimization procedure illustrated in Fig. 16 is carried out for all modulation strategies, considering nominal operating conditions. The same approach described in Fig. 17 is adopted, adjusting the switching frequency of each modulation strategy to achieve the same ΔI_{RMS} as the 2-L converter operated at 16 kHz. Once the switching frequency is selected, the minimum required chip area for each semiconductor device is identified and the converter losses are calculated. It is worth noting that this comparative evaluation is no longer independent of the converter power level and switching frequency (i.e., as opposed to the normalized comparison reported in Fig. 15), as the converter power level affects the conduction losses and the required chip size, while the selected switching frequency modifies the relative contribution of the switching losses to the total converter loss. Therefore, the results of this comparison do not have general validity but are specific for the considered converter specifications. Figure 18a, b and c shows the adjusted switching frequency f_{sw}, the required semiconductor chip area A_{S}, and the generated semiconductor loss P_{semi} for all modulation strategies, respectively. The figures also indicate the distribution between the 3-L SM and the 2-L inverter stages. The overall semiconductor efficiency η_{semi} is shown in Fig. 18d. As expected from the previous analysis (see Fig. 15), it is found that switching sequence *8* achieves the best performance in terms of converter losses and efficiency, while requiring the minimum semiconductor chip area. Again, switching sequence *S* achieves similar results to sequence *8* but remains less attractive, as it features larger variations in terms of $\Delta I_{\text{RMS}}(M)$ (see Fig. 11) and $E_{\text{sw}}(\varphi)$ (see Fig. 14).

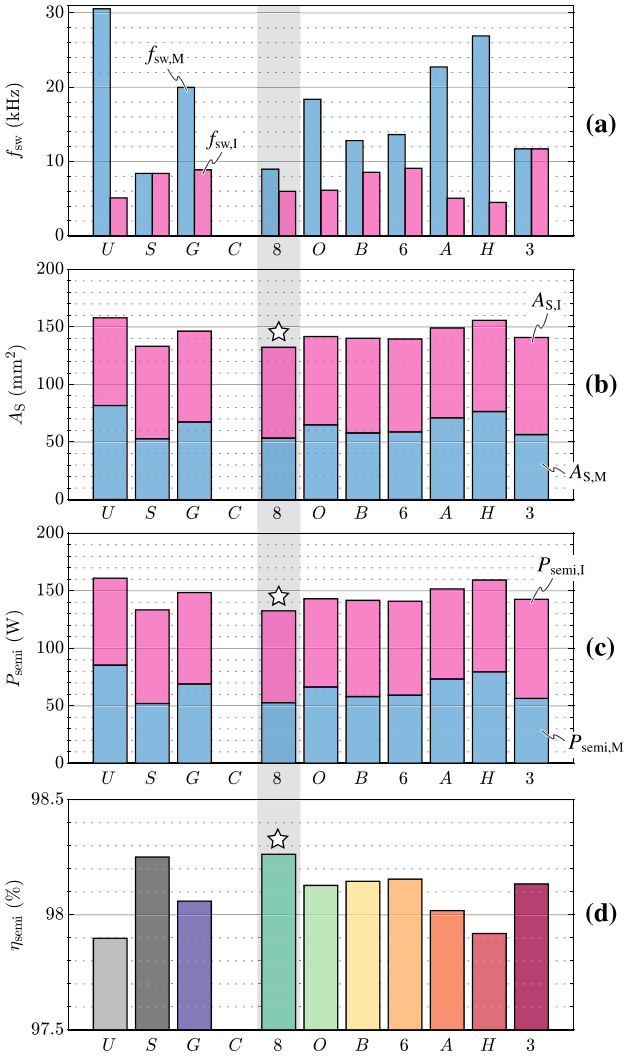

Fig. 18 Overview of the performance achieved by the 3-L SNPCC according to the chip area minimization procedure illustrated in Fig. 16 for different modulation strategies. $P = 7.5\,\text{kW}$, $V_{dc} = 800\,\text{V}$, $M = 0.85$ and $\cos\varphi = 1$ are considered (i.e., nominal operation). The switching frequency of each modulation strategy is adjusted to yield the same ΔI_{RMS} as the 2-L converter operated at 16 kHz, as in Fig. 17. **a** Switching frequency f_{sw}, **b** total semiconductor chip area A_S and **c** total semiconductor losses P_{semi}, divided between the 3-L SM and the 2-L inverter stages. **d** overall semiconductor efficiency η_{semi}. Sequence *C* is not present since $M > 1/\sqrt{3}$, while sequence *8* results the best performing in terms of minimum semiconductor chip area, minimum semiconductor loss and maximum converter efficiency ($\star$)

6 Conclusion

The SNPCC has not received much attention in literature so far, nevertheless it appears as a promising candidate for robust and cost-sensitive industrial drive applications, e.g. fans, pumps, etc., since it is able to generate a multi-level output voltage waveform adopting less active devices with respect to traditional 3-L converters.

This paper provides a complete investigation of the SNPCC operation, including a novel analysis of the DM and CM voltage formation process. Several modulation strategies are introduced according to a specific set of rules, including both symmetric and asymmetric pulse patterns. For each of these strategies, a complete analytical and/or numerical evaluation of the major component stresses is carried out, including the RMS ripple of the current supplied to the driven machine, the RMS current in the DC-link capacitors and the conduction/switching losses in the semiconductor devices. Based on the calculated stresses, the best performing modulation strategy for the application at hand is selected. Finally, considering a 7.5 kW 3-Φ system, the minimum semiconductor chip areas required by the 2-L, 3-L NPC and 3-L SNPC converters are investigated. It is found that the SNPCC requires the least total chip area below a defined switching frequency and offers comparable efficiency as the conventional 3-L NPC converter for the same harmonic current stress on the driven machine, resulting an excellent candidate for cost-sensitive low-frequency industrial drive systems.

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Appendix 1 Analytical RMS machine current ripple

The analytical derivation of the RMS current ripple through the inductive load of a 3-Φ 2-L converter is reported in [23]; a similar procedure is applied herein to the SNPCC, considering the RMS ripple of the current supplied to the driven machine. The local RMS current ripple can be obtained by integrating and averaging the ripple contributions of the three phases over a switching period $T_{sw} = 1/f_{sw}$ as

$$\Delta i_{RMS}^2 = \frac{1}{T_{sw}} \int_0^{T_{sw}} \frac{\Delta i_a^2 + \Delta i_b^2 + \Delta i_c^2}{3}\,\mathrm{d}t = \\ = \frac{1}{T_{sw}} \int_0^{T_{sw}} \frac{3}{2}\frac{\Delta i_\alpha + \Delta i_\beta}{3}\,\mathrm{d}t = \frac{1}{2}\Delta i_{\alpha\beta,RMS}^2, \qquad (39)$$

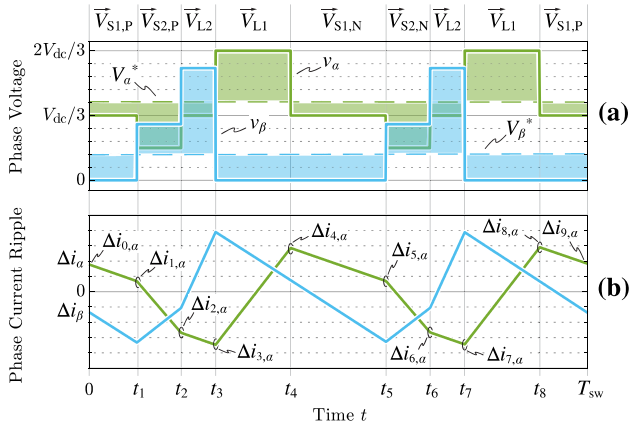

Fig. 19 Instantaneous waveforms considering a switching period in sector ① ($\vartheta = 15°$, cf. Fig. 2d), area Ⅱ ($M = 0.85$) and sequence *8* (cf. Table 3). **a** $\alpha\beta$ voltage waveforms and **b** $\alpha\beta$ current ripple waveforms. The distinctive behavior of the current ripple for asymmetric pulse patterns is shown, i.e. the ripple value is nonzero at the beginning, middle and end of the switching period

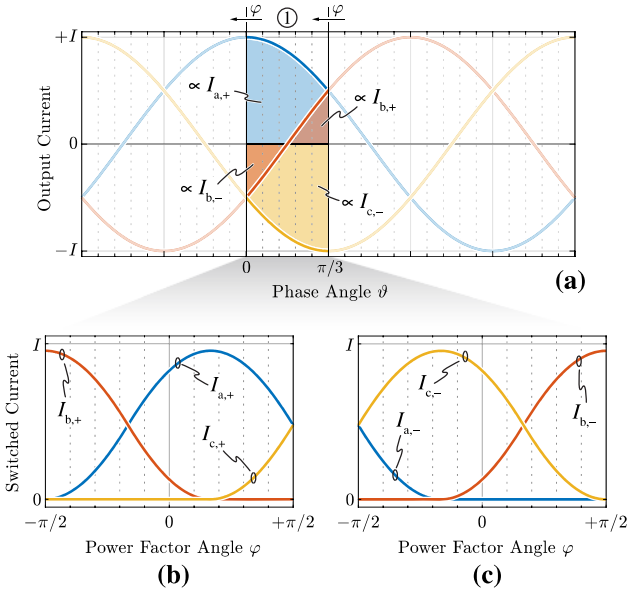

Fig. 20 **a** Overview of the positive/negative current averaging process in sector ①. Varying φ translates in shifting the averaging window. The results of the current averaging are divided between **b** positive contributions and **c** negative contributions changed in sign

where Δi_α and Δi_β are the current ripple components with respect to the $\alpha\beta$-axes defined in space vector theory. It is worth mentioning that symmetric pulse patterns are completely identified within half a switching period, however asymmetric sequences require the total period to be fully described. Therefore, the integration interval of (39) has been defined in the most general way.

The expressions of the instantaneous Δi_α and Δi_β can be obtained by integration of the high-frequency DM voltage component at the converter 3-Φ output, resulting in a piecewise linear function. Being N the total number of transitions in the switching sequence (i.e. 6, 8 or 10), the current ripple values at each state transition are defined as

$$\begin{cases} \vec{\Delta i}_{0,\alpha\beta} = -\vec{\Delta i}_{\alpha\beta,\mathrm{AVG}} \\ \vec{\Delta i}_{\mathrm{k},\alpha\beta} = \vec{\Delta i}_{\mathrm{k}-1,\alpha\beta} + \dfrac{\vec{V}_{\mathrm{k},\alpha\beta} - \vec{V}^*_{\alpha\beta}}{L}\delta_\mathrm{k} T_\mathrm{sw} \quad \mathrm{k} = 1,..,N+1 \end{cases} \tag{40}$$

where $\vec{V}_{\mathrm{k},\alpha\beta}$ is the applied space vector, $\vec{V}^*_{\alpha\beta}$ is the reference voltage vector, $\delta_\mathrm{k} T_\mathrm{sw}$ is the state dwell-time and L is the machine phase inductance. The main terms of (40) are illustrated in Fig. 19, considering sequence *8*. In order to obtain a current ripple waveform with zero average over a switching period, the starting value $\vec{\Delta i}_{0,\alpha\beta}$ must be equal to the ripple average changed in sign, which can be derived in a first iteration considering $\vec{\Delta i}_{0,\alpha\beta} = 0$ as

$$\vec{\Delta i}_{\alpha\beta,\mathrm{AVG}} = \frac{1}{2}\sum_{\mathrm{k}=1}^{N+1} \delta_\mathrm{k}\left(\vec{\Delta i}_{\mathrm{k}-1,\alpha\beta} + \vec{\Delta i}_{\mathrm{k},\alpha\beta}\right). \tag{41}$$

A zero current ripple average is already ensured by symmetric pulse patterns, but it is not guaranteed for asymmetric ones.

The RMS value of $\vec{\Delta i}_{\alpha\beta}$ can be calculated by exploiting its piece-wise linear properties:

$$\Delta i^2_{\alpha\beta,\mathrm{RMS}} = \frac{1}{3}\sum_{\mathrm{k}=1}^{N+1}\delta_\mathrm{k}\big[(\Delta i^2_{\mathrm{k}-1,\alpha} + \Delta i^2_{\mathrm{k},\alpha} + \Delta i_{\mathrm{k}-1,\alpha}\Delta i_{\mathrm{k},\alpha}) + (\Delta i^2_{\mathrm{k}-1,\beta} + \Delta i^2_{\mathrm{k},\beta} + \Delta i_{\mathrm{k}-1,\beta}\Delta i_{\mathrm{k},\beta})\big]. \tag{42}$$

Finally, substituting (42) in (39), the total RMS current ripple over one 3-Φ output period is obtained by averaging Δi^2_RMS over a single sector (i.e. 60°), as

$$\Delta I^2_\mathrm{RMS} = \frac{3}{\pi}\int_0^{\pi/3} \Delta i^2_\mathrm{RMS}\,\mathrm{d}\vartheta. \tag{43}$$

The presented procedure is here applied to sequence *8* for demonstration purposes, resulting in two different normalized expressions for area ① and area Ⅱ, respectively

$$\frac{\Delta I^2_{\mathrm{RMS},8①}}{\Delta I^2_\mathrm{n}} = \frac{M^2}{3}\left(M^2\frac{9}{8} + M\frac{8\sqrt{3}}{3\pi} + \frac{1}{2}\right) \tag{44}$$

$$\frac{\Delta I^2_{\mathrm{RMS},8\,\textcircled{II}}}{\Delta I^2_{\mathrm{n}}} = M^4\,\frac{3}{8} - M^3\,\frac{8\sqrt{3}}{3\pi} + M^2\left(\frac{29}{6} - \frac{5\sqrt{3}}{\pi}\right) + M\left[\frac{6\sqrt{3}}{\pi} - \frac{30\sqrt{3}}{\pi}\left(\frac{\ln(3)}{2} - \tanh^{-1}(\sqrt{3}-2)\right)\right] + \frac{14\sqrt{3}}{9\pi} - \frac{16}{27} \tag{45}$$

where ΔI_{n} is defined in (25).

Appendix 2 Analytical switching losses

To calculate the converter switching losses, the switched voltage V_{sw} and current i_{sw} values at each space vector transition (i.e. switching state change) must be known. It can be demonstrated that the total switching losses of both the 2-L inverter and the 3-L SM stages depend on the sequence starting vector and have sector periodicity, therefore the following analysis focuses only on sector ①. The current direction is of primary importance in determining whether the switching transition of a bridge-leg causes a hard turn-on or turn-off. Neglecting the switching frequency current ripple and adopting the simplified linear model reported in (33), the average converter switching energy loss can be calculated as

$$\frac{P_{\mathrm{sw}}}{f_{\mathrm{sw}}} = \frac{3}{\pi}\int_0^{\pi/3}\left(\sum_{\mathrm{j}=1}^{N} k_{\mathrm{j}}\, V_{\mathrm{sw,j}}\, i_{\mathrm{sw,j}}(\vartheta)\right)\mathrm{d}\vartheta, \tag{46}$$

where N is the number of transitions in the switching sequence (i.e. 6, 8 or 10) and k_{j} depends on the semiconductor technology of the device involved in the transition (i.e. different between the 2-L inverter and the 3-L SM) and on whether the transition causes a hard turn-on or turn-off (i.e. depending on the switched current direction). Since the instantaneous switched current can be either positive or negative, (46) can be expressed as

$$\begin{aligned}\frac{P_{\mathrm{sw}}}{f_{\mathrm{sw}}} &= \sum_{\mathrm{j}=1}^{N} V_{\mathrm{sw,j}}\left(\frac{3}{\pi}\int_0^{\pi/3} k_{\mathrm{j}}\, i_{\mathrm{sw,j}}(\vartheta)\,\mathrm{d}\vartheta\right)\\ &= \sum_{\mathrm{j}=1}^{N} V_{\mathrm{sw,j}}\left(k_{\mathrm{j},+}\, I_{\mathrm{sw,j},+} + k_{\mathrm{j},-}\, I_{\mathrm{sw,j},-}\right),\end{aligned} \tag{47}$$

where $I_{\mathrm{sw,j},+}$ and $I_{\mathrm{sw,j},-}$ are respectively the sector-averaged positive and negative (changed in sign) switched currents involved in the j-th transition, while $k_{\mathrm{j},+}$ and $k_{\mathrm{j},-}$ are the related switching loss coefficients (i.e. indicating either a turn-on or turn-off commutation). As the switched current can assume any of the 3-Φ sinusoidal output current values, 6 different $I_{\mathrm{sw,j}}$ terms are derived, i.e. the positive and negative averages of each 3-Φ sinusoidal output current inside sector ①.

The current averaging procedure and its results are illustrated in Fig. 20, however the analytical expressions are not reported for conciseness reasons. Moreover, Table 7 sum-

Table 7 Switched voltage and current values in sector ①, divided between area Ⓘ and area Ⓘ. The kind of hard commutation (turn-on or turn-off) and the involvement of the 3-L matrix (M) or the 2-L inverter (I) in the switching transition are indicated by the switching loss coefficient k

Area Ⓘ	V_{sw}	I_{sw}	k	Area Ⓘ	V_{sw}	I_{sw}	k
$\vec{V}_{\mathrm{Z1}} \rightarrow \vec{V}_{\mathrm{Z2}}$	0	$I_{\mathrm{b},+}$	$k_{\mathrm{on,I}}$	$\vec{V}_{\mathrm{L1}} \rightarrow \vec{V}_{\mathrm{L2}}$	V_{dc}	$I_{\mathrm{b},+}$	$k_{\mathrm{on,I}}$
		$I_{\mathrm{b},-}$	$k_{\mathrm{off,I}}$			$I_{\mathrm{b},-}$	$k_{\mathrm{off,I}}$
$\vec{V}_{\mathrm{Z1}} \leftarrow \vec{V}_{\mathrm{Z2}}$	0	$I_{\mathrm{b},-}$	$k_{\mathrm{on,I}}$	$\vec{V}_{\mathrm{L1}} \leftarrow \vec{V}_{\mathrm{L2}}$	V_{dc}	$I_{\mathrm{b},-}$	$k_{\mathrm{on,I}}$
		$I_{\mathrm{b},+}$	$k_{\mathrm{off,I}}$			$I_{\mathrm{b},+}$	$k_{\mathrm{off,I}}$
$\vec{V}_{\mathrm{S1}} \rightarrow \vec{V}_{\mathrm{S2}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{b},+}$	$k_{\mathrm{on,I}}$	$\vec{V}_{\mathrm{S1}} \rightarrow \vec{V}_{\mathrm{S2}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{b},+}$	$k_{\mathrm{on,I}}$
		$I_{\mathrm{b},-}$	$k_{\mathrm{off,I}}$			$I_{\mathrm{b},-}$	$k_{\mathrm{off,I}}$
$\vec{V}_{\mathrm{S1}} \leftarrow \vec{V}_{\mathrm{S2}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{b},-}$	$k_{\mathrm{on,I}}$	$\vec{V}_{\mathrm{S1}} \leftarrow \vec{V}_{\mathrm{S2}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{b},-}$	$k_{\mathrm{on,I}}$
		$I_{\mathrm{b},+}$	$k_{\mathrm{off,I}}$			$I_{\mathrm{b},+}$	$k_{\mathrm{off,I}}$
$\vec{V}_{\mathrm{Z1}} \rightarrow \vec{V}_{\mathrm{S1}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{a},+}$	$k_{\mathrm{on,M}}$	$\vec{V}_{\mathrm{L1}} \rightarrow \vec{V}_{\mathrm{S1}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{a},-}$	$k_{\mathrm{on,M}}$
		$I_{\mathrm{a},-}$	$k_{\mathrm{off,M}}$			$I_{\mathrm{a},+}$	$k_{\mathrm{off,M}}$
$\vec{V}_{\mathrm{Z1}} \leftarrow \vec{V}_{\mathrm{S1}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{a},-}$	$k_{\mathrm{on,M}}$	$\vec{V}_{\mathrm{L1}} \leftarrow \vec{V}_{\mathrm{S1}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{a},+}$	$k_{\mathrm{on,M}}$
		$I_{\mathrm{a},+}$	$k_{\mathrm{off,M}}$			$I_{\mathrm{a},-}$	$k_{\mathrm{off,M}}$
$\vec{V}_{\mathrm{Z2}} \rightarrow \vec{V}_{\mathrm{S2}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{c},-}$	$k_{\mathrm{on,M}}$	$\vec{V}_{\mathrm{L2}} \rightarrow \vec{V}_{\mathrm{S2}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{c},+}$	$k_{\mathrm{on,M}}$
		$I_{\mathrm{c},+}$	$k_{\mathrm{off,M}}$			$I_{\mathrm{c},-}$	$k_{\mathrm{off,M}}$
$\vec{V}_{\mathrm{Z2}} \leftarrow \vec{V}_{\mathrm{S2}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{c},+}$	$k_{\mathrm{on,M}}$	$\vec{V}_{\mathrm{L2}} \leftarrow \vec{V}_{\mathrm{S2}}$	$\frac{V_{\mathrm{dc}}}{2}$	$I_{\mathrm{c},-}$	$k_{\mathrm{on,M}}$
		$I_{\mathrm{c},-}$	$k_{\mathrm{off,M}}$			$I_{\mathrm{c},+}$	$k_{\mathrm{off,M}}$

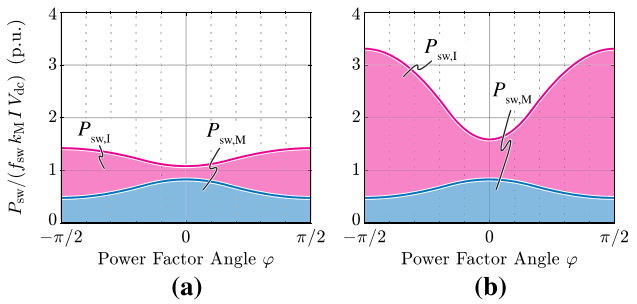

Fig. 21 Analytical switching losses for sequence *8* (cf. Table 3) in (a) area Ⓘ and (**b**) area Ⓘ. The loss expressions $P_{sw,M}$ and $P_{sw,I}$ are normalized by $f_{sw}\,k_M\,I\,V_{dc}$ and only depend on the k_I/k_M ratio (see Table 5)

marizes the switched current and voltage values involved in each space vector transition, together with the kind of hard commutation (i.e. turn-on or turn-off) and the semiconductor technology of the device being switched, i.e. $k_{on,M}/k_{off,M}$ for the 3-L SM devices and $k_{on,I}/k_{off,I}$ for the 2-L inverter devices.

Considering the switching sequence mirroring process between odd and even sectors described in Sect. 3, it is found that each converter bridge-leg transition is repeated in the same direction in the diametrically opposite sector (i.e. at $\vartheta + 180°$), however the switched current value is changed in sign. Therefore, simplified expressions of the 3-L SM and 2-L inverter switching losses are derived by averaging the loss contributions of both sequence combinations, obtaining

$$P_{sw,M} = \frac{1}{2}\, f_{sw} \sum_{j=1}^{N_M} k_M\, V_{sw,j} \left(I_{sw,j,+} + I_{sw,j,-}\right), \tag{48}$$

$$P_{sw,I} = \frac{1}{2}\, f_{sw} \sum_{k=1}^{N_I} k_I\, V_{sw,k} \left(I_{sw,k,+} + I_{sw,k,-}\right), \tag{49}$$

where N_M and N_I are respectively the number of switching transitions involving the 3-L SM and the 2-L inverter, while $k_M = k_{on,M} + k_{off,M}$ and $k_I = k_{on,I} + k_{off,I}$ are the total switching loss coefficients. Leveraging (48) and (49), together with the semiconductor device parameters reported in Table 5, it is possible to analytically derive the switching losses for all modulation strategies. The resulting expressions for sequence *8* are here reported for demonstration purposes, divided between the 3-L SM contribution

$$P_{sw,M,8} = f_{sw}\, k_M\, I\, V_{dc} \begin{cases} \dfrac{3\sqrt{3}\cos\varphi}{2\pi} & |\varphi| \le \dfrac{\pi}{6} \\ \dfrac{3(2-\sin|\varphi|)}{2\pi} & \dfrac{\pi}{6} < |\varphi| \le \dfrac{\pi}{2} \end{cases}, \tag{50}$$

which is independent on the sector area, and the 2-L inverter contribution in area Ⓘ and area Ⓘ, respectively

$$P_{sw,I,8\,Ⓘ} = f_{sw}\, k_I\, I\, V_{dc} \begin{cases} \dfrac{3(1-\sqrt{3}\cos\varphi)}{2\pi} & |\varphi| \le \dfrac{\pi}{6} \\ \dfrac{3\sin|\varphi|}{2\pi} & \dfrac{\pi}{6} < |\varphi| \le \dfrac{\pi}{2} \end{cases}, \tag{51}$$

$$P_{sw,I,8\,Ⓘ} = f_{sw}\, k_I\, I\, V_{dc} \begin{cases} \dfrac{3(6-3\sqrt{3}\cos\varphi)}{2\pi} & |\varphi| \le \dfrac{\pi}{6} \\ \dfrac{9\sin|\varphi|}{2\pi} & \dfrac{\pi}{6} < |\varphi| \le \dfrac{\pi}{2} \end{cases}. \tag{52}$$

The obtained expressions are characterized by a 180° periodicity with respect to the power factor angle φ and are graphically reported in normalized form in Fig. 21.

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